REMARKS

In response to the Office Action of August 4, 2003, Applicant proposes to amend his application and requests reconsideration in view of the proposed amendment and following remarks. It is not proposed in this Amendment to add or cancel any claims so that, upon entry of the Amendment, claims 1-8 and 13-16 remain pending.

In the Official Action, claims 1-4 were rejected as unpatentable over Ma et al. (U.S. Patent 5, 939,753, hereinafter Ma) in view of Chang et al. (published U.S. patent application 2002/0086467, hereinafter Chang). This rejection is respectfully traversed.

The rejection is legally incorrect because Chang is not prior art pursuant to U.S. law. Chang is a published U.S. patent application, which has as its effective date its U.S. filing date, December 28, 2000. Although the present patent application was not filed until July 25, 2001, it claims the priority of Japanese patent application 2000-287419 filed September 21, 2000. In order to perfect that priority, pursuant to 37 CFR 1.55(a)(4), Applicant submits a certified English language translation of the Japanese patent application from which priority is claimed. Claims 1-4 are supported in the translation, pursuant to 35 USC 112, first paragraph, at page 16, lines 7-12, from page 19, line 24 to page 20, line 12, page 34, lines 3-10, page 38 line 22 to page 39, line 3, and in Figure 10. Thus, upon the filing of the attached translation, Chang must be withdrawn as a reference and, therefore, the rejection is overcome. Accordingly, claims 1-4 should now be allowed.

Dependent claims 7, 8, 14, and 15 were indicated as allowable. No further comment on these claims is necessary.

In this Amendment independent claims 5, 6, 13, and 16 are similarly amended. In these claims the first and second polysilicon layers from which different electrodes are made have at least one of different dopant impurity concentrations and thicknesses. Because of these asymmetries in these layers, improved reliability is achieved, as described in the patent application from page 37, line 21 through page 38, line 2.

The invention as defined by independent claims 5, 6, 13, and 16, concerns a high-frequency semiconductor device including an MOS transistor on a substrate, a first lateral polysilicon diode on the substrate that provides electrostatic discharge (ESD) protection, and a capacitor with polysilicon electrodes that aids in providing that ESD protection. The first lateral polysilicon diode and the lower electrode of the capacitor are formed from the same polysilicon layer. The MOS transistor has a polysilicon gate made from a different polysilicon layer than the polysilicon layer shared by the first lateral polysilicon diode and the lower electrode of the capacitor. In some claimed structures, that gate is made from the same polysilicon layer that forms the other electrode of the capacitor. The fact that these two

polysilicon layers have different dopant concentrations and or different thicknesses provides very important advantages in the invention.

Polysilicon gate electrodes of MOS transistors must have a sufficiently high doping impurity concentration for low voltage operation of the MOS transistor. If the dopant impurity concentration is insufficient, the gate electrode may be depleted of charge carriers when a gate voltage is applied. As known to those of skill in the art, a region depleted of charge carriers is a high resistance region producing a significant voltage drop that prevents high-frequency operation of the transistor with a low voltage. On the other hand, when the dopant concentration of polysilicon is relatively high, the number of defects in the polysilicon layer increases. These defects contribute to early failure of the polysilicon layer and associated diode. Therefore, there are competing interests in determining the dopant concentration of the gate electrode, i.e., reliability versus low resistance. For that reason it is inappropriate to make a polysilicon gate electrode of an MOS transistor from the same layer from which a polysilicon diode is made.

In addition, it is desirable to make a polysilicon layer used as a gate electrode of an MOS transistor relatively thick to avoid the effects of impurity absorption in the manufacturing process. If the impurity is boron, for example, the boron may be absorbed into the gate insulating layer just opposite the gate electrode. When that absorption occurs, the reliability of the transistor is seriously degraded. On the other hand, in the lateral polysilicon diode, the thickness of the polysilicon layer is of substantial importance because of the lateral operation of the diode. When, as in the invention, dopant impurities are introduced by ion implantation, the concentration of the implanted impurity varies in the depth direction of the polysilicon layer. Thus, the diode characteristic is not uniform in the depth direction of the substrate. To minimize that non-uniformity and its effects, it is important that the polysilicon layer be relatively thin. Again, there are competing considerations in the thickness of the polysilicon layer, i.e., it should be thick to function well as the gate electrode of the transistor and should be thin to avoid variations in doping concentrations with depth.

Based upon the foregoing considerations, it is important to form the polysilicon layers of the gate electrode of the transistor and of the lateral polysilicon diodes from different polysilicon layers. The invention takes advantage of the fact that an additional polysilicon layer is employed as one of the electrodes of the capacitor, the electrode identified as the lower electrode in the claims. The constraints on a desirable polysilicon layer as a capacitor electrode are far more relaxed then those for the gate electrode and the lateral polysilicon diode. Thus, by establishing at least one of the differences in dopant concentration and thickness mentioned in the amendments to independent claims 5, 6, 13, and 16, the reliability

and performance of the claimed high frequency semiconductor device is improved without a significant manufacturing cost increase.

Claims 5, 6, 13, and 16, as examined, were rejected as unpatentable over Ma et al. (U.S. Patent 5,939,753, hereinafter Ma) in view of Wang (U.S. Patent 6,351,353). This rejection is respectfully traversed.

The secondary reference, Wang, was relied upon as describing an ESD circuit including diodes. The only figure within Wang showing any kind of a structure that might relate to the amended claims, and their amendment, is Figure 1B. However, that figure and its description provide no disclosure of or even suggestion for the limitation added to each of the four amended independent claims. Thus, unless Ma includes that disclosure, the combination of references cannot establish *prima facie* obviousness of any of claims 5, 6, 13, and 16.

There is no description within Ma with regard to Figures 8 and 10, the figures referred to by the Examiner, as to the relative thicknesses and dopant concentrations of the two polysilicon layers 44 and 56 that form the electrodes of a capacitor that includes a dielectric layer 45. The layer 44 seems to be formed simultaneously with the layer that becomes the gate electrodes 53-55. As to the relative thicknesses, some differences are apparent from Figures 8 and 10, but there is no indication that those figures are drawn to scale. For that reason, it is not proper to assume that the depicted thickness relationship constitutes any disclosure of relative thicknesses of layers. Further, without a disclosure concerning relative thicknesses and/or dopant concentrations, it is not possible for Ma to establish *prima facie* obviousness, even considered in combination with Wang, as to the amended claims 5, 6, 13, and 16. Accordingly, upon reconsideration, the rejection of those claims should be withdrawn

The foregoing amendment places the application in form for allowance so that the Amendment should be entered and the application should be allowed.

Respectfully submitted,

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Date: November 3, 2003
JAW/tps

VERIFICATION OF TRANSLATION

I, Mochikazu Hori, being a citizen of Japan, residing at c/o ASAHINA & CO., NS Bldg., No. 2-22, Tanimachi 2-chome, Chuo-ku, Osaka-shi, Osaka, 540-0012, Japan, do solemnly and sincerely declare as follows:

I am a translator, of ASAHINA & CO., of NS Bldg., No. 2-22, Tanimachi 2-chome, Chuo-ku, Osaka, 540-0012, Japan.

I am well acquainted with the English and Japanese languages.

The attached translation is a true and correct translation into the English language of a certified copy of Japanese Patent Application No. 2000-287419 filed on September 21, 2000.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

This 28th day of October, 2003

by Mochikazu Hori

Mochikazu Hori

PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Patent Application Number: 2000-287419

Applicant: Mitsubishi Denki Kabushiki Kaisha

March 9, 2001

Commissioner, Patent Office Kozo Oikawa

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SPECIFICATION

[Title of the Invention]

Si-MOS HIGH-FREQUENCY SEMICONDUCTOR DEVICE AND THE MANUFACTURING METHOD OF THE SAME

[CLAIMS]

1. A high-frequency semiconductor device comprising a Si MOS transistor and a lateral polysilicon diode both formed on a substrate, wherein said lateral polysilicon diode is obtained by forming PN junction on the substrate,

wherein the lateral polysilicon diode connects a high-frequency I/O signal line and an externally supplied voltage VDD, and forward direction of the lateral polysilicon diode is a direction from the high-frequency I/O signal line to the externally supplied voltage VDD.

2. A high-frequency semiconductor device comprising a Si MOS transistor and a lateral polysilicon diode both formed on a substrate, wherein said lateral polysilicon diode is obtained by forming PN junction laterally on the substrate,

wherein the lateral polysilicon connects diode ground GND and a high-frequency I/O signal line, and forward direction of the lateral polysilicon diode is a direction from the ground GND to the high-frequency I/O signal line.

3. A high-frequency semiconductor device comprising a Si

MOS transistor and a lateral polysilicon diode both formed on a substrate, wherein said lateral polysilicon diode is obtained by forming PN junction laterally on the substrate,

wherein the lateral polysilicon diode connects a high-frequency I/O signal line and an externally supplied voltage VDD, and forward direction of the lateral direction is a direction from the high-frequency I/O signal line to the externally supplied voltage VDD, said high-frequency semiconductor device further comprising a lateral polysilicon diode on the substrate, wherein said lateral polysilicon diode is obtained by forming PN junction laterally on the substrate, wherein the lateral polysilicon diode connects ground GND and a high-frequency I/O signal line, and forward direction of the lateral polysilicon diode is a direction from ground GND to the high-frequency I/O signal line.

4. A high-frequency semiconductor device comprising a Si MOS transistor and a lateral polysilicon diode both formed on a substrate, wherein said lateral polysilicon diode is obtained by forming PN junction laterally on the substrate,

wherein the lateral polysilicon diodes of a number "m" are connected between a high-frequency I/O signal line and an externally supplied voltage VDD in series, and forward direction of the lateral direction is a direction from the high-frequency I/O signal line to the externally supplied voltage VDD, said high-frequency semiconductor device further comprising lateral polysilicon diodes on the substrate, wherein the lateral polysilicon diodes of a number "n" are connected between ground GND and a high-frequency I/O line in series, and with assuming the voltage of VDD as V_{dd}, $V_{dd}/(n+m)$ is smaller than 1.1 (V).

5. A high-frequency semiconductor device of any one of Claims 1, 2, 3 and 4, wherein a lateral polysilicon diode is not connected to a signal line other than a high frequency I/O signal line.

6. A high-frequency semiconductor device of any one of Claims 1, 2, 3, 4 and 5 further comprising a capacitor having a lower electrode and an upper electrode both formed with polysilicon, wherein the lateral polysilicon diode and the lower electrode of the capacitor are formed from same polysilicon layer, and gate electrode of the MOS transistor is formed from another polysilicon layer.

7. A high-frequency semiconductor device of any one of Claims 1, 2, 3, 4 and 5 further comprising a capacitor having a lower electrode and an upper electrode both formed with polysilicon, wherein the lateral polysilicon diode and the lower electrode of the capacitor are formed from same polysilicon layer, and gate electrode of the MOS transistor and the upper electrode of the capacitor are formed from same polysilicon layer as that of the upper electrode of the capacitor.

8. A high-frequency semiconductor device of claim 6 or 7, wherein polysilicon layer to form the upper electrode of the capacitor and/or a dielectric layer of the capacitor is also left on and covering PN junction of the lateral polysilicon diode.

9. A manufacturing method of high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes and a capacitor on a substrate, and the lateral polysilicon diode connects a

high-frequency I/O signal line and externally supplied voltage VDD, and the other lateral polysilicon diode connects ground GND and the high-frequency I/O signal line;

wherein the lower electrode of the capacitor and the lateral polysilicon diode are formed from a first polysilicon layer,

the insulating film of the capacitor is formed from a first dielectric layer,

the upper electrode of the capacitor is formed from a second polysilicon layer,

the first dielectric layer and/or the second polysilicon layer is/are left on a certain region of the first polysilicon layer at which PN junction of the lateral polysilicon diode is to be formed, and

an edge of a resist mask used for injecting ion into N-type region of the lateral polysilicon diode and an edge of a resist mask used for injecting ion into the P-type region of the lateral polysilicon diode are placed on the first dielectric layer and the second polysilicon layer being left.

10. A manufacturing method of claim 9, wherein gate electrode of the MOS transistor is formed from the second polysilicon layer.

11. A high-frequency semiconductor device of claim 1 further comprising a clamp circuit connected between the externally supplied voltage VDD and the ground GND, wherein the clamp circuit operates to flow current within voltage lower than the absolute value of reverse bias breakdown voltage of the lateral polysilicon diode.

[DETAILED DESCRIPTION OF THE INVENTION]

[Technical Field of the Invention]

The present invention relates to a high-frequency semiconductor device employing a Si-MOS transistor, and especially relates to achievement of reliable and sophisticated high-frequency semiconductor device having a high ESD (Electro Static Discharge) resistance.

[Prior Art]

Mobile phone and wireless LAN are widespread in application in recent years, so a high-frequency semiconductor device, which is necessary in electric devices of these uses to improve their performance, size and costs, has been spotlighted. To achieve above the high-frequency semiconductor device, III-V group compound semiconductor such as GaAs with high electron mobility is mainly used. However, with minimizing a Si-MOS transistor rapidly in recent years, it becomes possible to form a MOS(Metal-Oxide-Semiconductor) transistor of the gate length 0.2 μm or less, thereby transconductance Gm of a MOS transistor is greatly improved so that high-frequency characteristics thereof is improved and becomes applicable to high-frequency device for GHz band. The invention achieves a reliable and sophisticated high-frequency semiconductor device having the high ESD (Electro Static Discharge) resistance with employing MOS transistor of Si.

A phenomenon in which electrostatically charged object contacts with other object(s) and causes electrical discharge is called an ESD (Electro Static Discharge). The phenomenon happened at semiconductor device may destroy semiconductor elements. As theoretic models of the ESD, discharge models of an HBM (Human Body

Model) presenting discharge from electrically charged human body to semiconductor elements, an MM (Machine Model) presenting discharge from electrically charged machine to semiconductor element, and a CDM (Charge Device Model) presenting discharge from charged semiconductor itself to grounded object are well-known. The current waveforms of the HBM and the CDM are shown in FIG. 1. In the figure, a current of approximately 1 A is caused for relatively long time (to 100 ns) in HBM and on the other hand, a large current of approximately 10 A is caused for a very short time (to 1 ns) in the CDM.

As mentioned above, in case of ESD, impressing large current into the semiconductor element in a short time result in melt-down of the element due to heat caused by joule loss (this is referred as thermal destruction). Moreover, in case high voltage caused by the ESD is applied to gate insulting layer of the MOS transistor, which is typically and widely used in recent Si-LSI (Large-Scaled Integration) device, breakdown of the gate insulting layer may be caused. Accordingly, these kinds of device destruction caused by the ESD, i.e. thermal destruction and breakdown of insulation, are problematic.

In order to prevent these destruction, various protection circuits are typically formed into the semiconductor device between internal circuit on a Si wafer and I/O pins so as not to transmit high voltage surge due to the EDS to the internal circuit. Since the I/O pins are connected to I/O pads on the wafer through wire bonding, protection circuits are typically formed between the internal circuit and the I/O pads. Anyway, these protection circuits are commonly used and called as the ESD protection circuits.

As the ESD protection circuits, circuit wherein the MOS

transistors in OFF state are connected to I/O signal line is often used as referred in the article by M-D.Ker et.al., "IEDM, pp.889-892, 1996" (hereinafter article 1) for example. FIG. 2 is a circuit diagram illustrating typical ESD protection circuit. As shown in the figure, drain of N-type MOS transistor (hereinafter referred as an NMOS) 31 wherein gate, source and P-well thereof are grounded and drain of P-type MOS transistor (hereinafter referred as a PMOS) 32 wherein gate, source and N-well thereof are connected to external supply voltage (hereinafter referred as VDD) are connected to the I/O signal line connecting the I/O pad 30 and the internal circuit 100. Since the MOS transistor 31 and 32 are both in OFF state, no current can flow through these transistors and give no effect on operation of the semiconductor device ordinarily. When a surge due to the ESD is impressed from the I/O pad 30, parasitic bipolar transistor action shall be occurred in either of these transistors to form path for flowing, i.e. dispersing, large current from the drain to the source thereof.

With referring to FIG. 3, the parasitic bipolar transistor action of the MOS transistor will be described. It is assumed that surge 45 of positive voltage enters into the drain of the NMOS 31 in here. First of all, a positive voltage of the surge is impressed to N+ diffusion layer 313 of drain. When the positive voltage of surge is increased, PN junction of N+ diffusion layer 313, which is reversely biased with this surge, causes breakdown and impact ionization occurs to generate a large amount of pair of electron and hole. Among generated pairs of electron and hole, the electron flow into the drain of positive voltage and the hole shall flow into grounded P-well 314. With presenting current owing to the flowing holes as I_{hole}, and resistance of the P-well as R_{sub}, the

voltage difference of $I_{hole} \cdot R_{sub}$ shall appear in the depth direction within the P-well 314, thereby electric potential of P-well region 350 directly below a gate 311 of the NMOS increases positively. At this time, in the NPN parasitic bipolar transistor comprising the N+ diffusion layer 313 of drain, P-well region 350 directly below the gate and the N+ diffusion layer 312 of source, junction between the N+ diffusion layer 313 of drain and P-well region 350 is reversely biased and junction between the P-well region 350 and the N+ diffusion layer 312 of source is forwardly biased, thereby turning ON the NPN parasitic bipolar transistor. As described above, although the NMOS 31 is ordinarily in OFF state because the gate 311 is grounded, the positive voltage of ESD surge 45 turns ON the NPN parasitic bipolar so that large current can be flown as shown with arrow 333. In addition, the positive voltage of surge is also applied to the drain of PMOS 32 and biases diode junction between the drain and N-well forwardly, thereby the diode junction is turned ON to disperse a current to the N-well.

Similarly, when the ESD of negative voltage is impressed to the I/O pad 30, parasitic bipolar of the PMOS 32 is turned ON to disperse a large current to the VDD. The negative voltage of surge is also applied to the drain of the NMOS 31 and turns ON a diode junction between the drain and P-well to disperse a current into the P-well.

Thus, with using the ESD protection circuit employing MOS transistor in OFF state can disperse a large current to the GND and the VDD so as to prevent thermal destruction and breakdown of the gate insulating layer with preventing that large current enters into internal circuit.

In order to accomplish the good ESD protection by the MOS

transistors in OFF state, it is well known that layout of the MOS transistors should be noted. That is, in the MOS transistors for the ESD protection, sufficient distance between gate electrode 60 and contact 63 connected to source or drain diffusion layer is required, i.e. certain distance 65 between gate and contact must be maintained as shown in FIG. 4. According to the article 1 by M-D.Ker et.al., the required distance 65 between gate and contact is 5 to 6 μm. With assuming the distance 65 between gate and contact to be "d", the diameter of the contact 63 to be "c", the width of source region 61 and drain region 62 situated between the gate electrodes 60 is obtained by an equation of "2d+c". Since it is required to take the distance 65 between gate and contact enough in the MOS transistor used as ESD protection element, the width of the source region 61 and the drain region 62 shall become larger. For example, in the design rule of 0.2 μm, typical diameter "c" of the contact 63 is approximately 0.2 μm, therefore, the width of the source region 61 and the drain region 62 obtained by "2d+c" is very large such as 10.2 to 12.2 μm. Moreover, in order to achieve sufficient ESD protection, the width, which appears in up and down direction in FIG.4, of the gate of the MOS transistor should be at least 100 μm or more. In the design rule of 0.2 μm, parasitic capacitances of source/drain diffusion layer, i.e. depletion layer capacity of PN junction between source/drain diffusion layer and well, is commonly 1 fF/μm^2. Therefore, in the MOS transistor used as the ESD protection element, parasitic capacitances of the source/drain diffusion layers for Si substrates, that is wells, is very large, such as 1.02 to 1.22 pF.

This large parasitic capacitances of the ESD protection

element had not been a problem in a semiconductor memory and a semiconductor logic device, however, it causes serious problem in the high-frequency semiconductor device using Si-MOSes. That is, since an impedance $|z|$ due to capacitance C is presented by $1/(2 \pi fC)$, the larger a frequency "f" becomes, i.e at high frequency, the smaller the impedance $|z|$ becomes. When the capacity "C" further increases, impedance $|z|$ of the capacity "C" is to be further reduced. That is, in a case where large capacitance of the drain diffusion layer is connected to high-frequency I/O signal line, the impedance due to this drain diffusion layer capacitance becomes very small.

As shown in the article of R. Groves "IEEE BCTM pp.149-152, 1999" (hereinafter article 2), high quality semiconductivie substrates having high resistivity such as substrates used for semiconductor device of GaAs compound are hardly available in Si semiconductor device. Accordingly, substrates of relatively low resistance are employed in Si semiconductor device. Therefore, in case of connecting ESD protection elements to the high-frequency I/O signal line as equivalent circuit in FIG. 5, the capacitance of drain diffusion layers in ESD protection element 33 and 34 are large so that the impedance at high frequency is very small. Moreover, due to that resistances 35 and 36 of Si substrate to which the capacitance 33 and 34 are connected are also small, most of high frequency signal S_1 on the high-frequency I/O signal line flow into the ESD protection element and are dispersed into the resistance of Si substrate.

As mentioned above, it has not been possible in the prior art to achieve a sophisticated and highly reliable high-frequency Si-MOS semiconductor device having the high ESD resistance through forming

ESD protection element.

[Problems to be Solved by the Invention]

The present invention provide a sophisticated and highly reliable high-frequency Si-MOS semiconductor device having high ESD resistance.

[Means to Solve the Problems]

A high-frequency semiconductor device according to one embodiment of the present invention is characterized in that lateral polysilicon diodes are connected between high-frequency I/O signal line and external power supply VDD, and between ground GND and the high-frequency I/O signal line respectively, and forward direction of the lateral polysilicon diode is direction from the high-frequency I/O signal line to the external supply voltage VDD, and from the ground GND to the high-frequency I/O signal line respectively.

A high-frequency semiconductor device according to another embodiment of the present invention is characterized in that lateral polysilicon diodes to the number of "m" are connected between the high-frequency I/O signal line and externally supplied voltage VDD in series, and lateral polysilicon diodes to the number of "n" are connected between the ground GND and the high-frequency I/O signal line in series, and forward direction of lateral polysilicon diode is direction from the high-frequency I/O signal line to the external supply voltage VDD and from the GND to the high-frequency I/O signal line, and with assuming the voltage of VDD as V_{dd} ,V_{dd} /(n+m) is preferably smaller than 1.1[V].

A high-frequency semiconductor device according to still other embodiment of the present invention is characterized in that at

least a MOS transistor, a dielectric film of capacitor and a lateral polysilicon diode are provided on its substrate, and wherein the lateral polysilicon diodes are formed from the same polysilicon layer as a lower electrode of the capacitor, and wherein a gate electrode of MOS transistor is formed from another polysilicon layer. The gate electrode of the MOS transistor may be formed from the same polysilicon layer as the upper electrode of the capacitor.

A high-frequency semiconductor device according to still further embodiment of the present invention is characterized in that dielectric film of the capacitor or/and polysilicon layer used for upper electrode of the capacitor are left on and covering a PN junction of lateral polysilicon diodes, and edges of resist pattern used for injecting ion into the lateral polysilicon diodes are placed on the dielectric film or/and polysilicon layer on the PN junction.

A high-frequency semiconductor device according to further still other embodiment of the present invention is characterized in that a clamp circuit connected between the externally supplied voltage VDD and ground GND, wherein the clamp circuit operates to flow current within voltage lower than the absolute value of reverse-breakdown voltage of the lateral polysilicon diodes.

[Embodiment for carrying out the Invention]

[EMBODIMENT 1]

FIG. 6 shows arrangement of ESD protection circuit for the high-frequency semiconductor device according to the present invention. FIG. 7 shows the structure of ESD protection element. In the ESD protection circuit according to the present embodiment, the lateral

polysilicon diodes, which are formed with polysilicon (polycrystal silicon layer) for forming gate electrodes of the Si-MOS transistor, are employed. By the lateral polysilicon diodes, the clamp circuit for ESD is composed.

ESD protection through clamp circuit employing diodes is well known, hereinafter the function will be described. Diode 38 is connected between signal line, which connects an I/O pad 30a and an internal circuit 100, and VDD (positive voltage supplied externally). The forward direction of the diode 38 is the direction from the signal line to the VDD as shown in FIG.6 (a). Further, another diode 37 is connected between GND and the signal line. The forward direction of the diode 37 is the direction from the GND to the signal line. When a positive voltage higher than VDD flows into the signal line in this diode clamp circuit, a diode 38 to which VDD is connected shall be turned ON and disperse the current toward the VDD. Until voltage of the signal line becomes lower than VDD, the diode 38 maintains its ON state. On the contrary, when a negative voltage lower than GND flows into the signal line, the diode 37 to which GND is connected shall be turned ON and disperse the current toward the GND. The diode 37 keeps ON state until a voltage of the signal line becomes higher than the GND. Thus, the clamp circuit can limit the voltage. Therefore, a positive high voltage ESD surge 45a impressed to the signal line shall be dispersed to the VDD via the diode 38(FIG.6 (b)). On the other hand, a negative high voltage ESD surge 45b impressed to the signal line is dispersed to the GND via the diode 37 as shown in FIG.6(c), thereby preventing the destruction of the internal circuit 100, to which the signal line is connected, from the ESD.

According to the article by A.Z.Wang et.al. "IEEE BCTM

pp.46 to 49. 1999" (hereinafter article 3), the clamp circuit employing diodes also has serious disadvantages. In a case where the voltage of VDD is impressed to the signal line at normal operation wherein no ESD is occurred, the voltage of the signal line may be certain higher than VDD due to that supplied VDD varies (Normally, variation of ± 10 % is permitted in the industrial standard). In this case, the diode connected to VDD is turned ON, and a large leakage current flows through the diode. Therefore, it was difficult to use the clamp circuit employing diode for ESD protection.

Next, the description of lateral polysilicon diodes which is employed in the present invention is given. As shown in the FIG. 7, the lateral polysilicon diodes is made by forming PN junction laterally with forming P-type region 85 and N-type region 86 by injecting ion into a polysilicon film 84 which is formed on an insulating layer 82 of silicon oxide. As presented in the article by M.Dutoit et.al. "J. Electrichem. Soc. Vol.125, No.10, pp.1648 to 1651,1978" (hereinafter article 4), lateral polysilicon diodes has been studied since 1970's. Other than the article 4 by M.Dutoit et.al., many studies has been done. As an example of application to the semiconductor device, the article of Y.Miyawaki et.al. "IEEE J. Solid-State Circuits, vol.34, pp.1551 to 1556, Nov.1999" (hereinafter article 5) in which step-up circuit of flash memory which is a nonvolatile memory is enumerated. As shown in the study examples, lateral polysilicon diodes have an advantage that their parasitic capacitances is small because they are isolated from the Si substrates by the insulating layer of silicon oxide or the like. In the application to the step-up circuit of the flash memory shown in the article 5, a high efficiency step-up circuit is achieved with taking an

advantage that there is no body effect with the lateral polysilicon diodes. Although the lateral polysilicon diodes have such advantages, they also have a serious problem as revealed in the many researches. That is, unlike to monocrystal silicon, polysilicon has a lot of defects and large grain size so that deep trap of energy level is formed and a reverse bias leakage current 72 is very large as shown in FIG. 8. In FIG.8, forward bias leakage current 71 is also shown for reference. Though the monocrystal silicon shows ideal diode characteristics, since large current is leaked as shown in FIG.8, the lateral polysilicon diodes could not be applied for a semiconductor logic device in which lower power consumption and lower leakage current are required. It was not also possible to apply to the semiconductor logic device because the leakage current causes mis-operation such as inversion between "1" and "0". Further, a problem concerning with durability is critical. Polysilicon, which has a lot of defectives by nature of polycrystal, was not ensure reliability for enduring ON/OFF switching frequencies expected in life of ten years as typical semiconductor devices. Therefore, the lateral polysilicon diodes can not be applied to the logic device in view of reliability. In the article 5, lateral polysilicon diodes are applied not to a general circuit of the flash memory but to the step-up circuit. In the step-up circuit, large leakage current of lateral polysilicon diodes is not problematic. Moreover, the step-up circuit only operates during writing and deleting of the flash memory, so that frequencies of ON/OFF switching is several digits fewer than that of typical semiconductor device. Only for the step-up circuit supporting these conditions, the lateral polysilicon diodes can be applicable.

As described above, it was difficult to use a diode, especially a

lateral polysilicon diode, as an element for the ESD protection circuit conventionally. The present invention is directed to solve these problems in the prior art through the following methods, and achieve a sophisticated and highly reliable semiconductor device having high ESD resistance in the high-frequency device employing with Si-MOS transistor for the first time.

In the present invention, a clamp circuit which employs lateral polysilicon diodes as ESD protection elements is attached only to high-frequency I/O signal line among all I/O signal lines of the high-frequency device employing with Si-MOS transistor. The prior art ESD protection circuit may be attached to other signal line with no high-frequency signals.

In the high-frequency I/O signal line, the DC bias voltage can be set to any preferable voltage. Therefore it is possible to apply certain voltage between VDD and GND instead of VDD as the DC bias voltage. By designing a bias circuit in such manner, a voltage of signal line shall not become higher than VDD even if VDD varies. As a result, a problem discussed in the article 3 in which diode is turned ON due to the variation of VDD in the clamp circuit employing diode can be solved. Therefore, the clamp circuit employing with diodes can be applied for the ESD protection.

Moreover, the high-frequency I/O signal line to which the lateral polysilicon diodes is connected supplies only bias voltage as DC circuit operation, therefore it shall not cause mis-operation even if a large reverse bias leakage current flows through the lateral polysilicon diodes. Therefore, the reverse bias leakage current in the lateral polysilicon diodes has not cause a problem so that the lateral polysilicon

diodes can be used as protection element of clamp circuit. Though the bias voltage on the high-frequency circuit varies depend on the reverse bias leakage current, the bias voltage can be set with assuming this variation caused by the reverse bias leakage current. Thus, a large reverse bias leakage current of the polysilicon diode has no influence on the high-frequency characteristic of the signal line and the internal circuit at all, thereby preventing mis-operation to realize highly reliability. Again it should be noted, as mentioned above, lateral polysilicon diodes could not be used as a protection element for clamp circuit in the logic device that operates at DC voltage.

The ESD protection element operates only when ESD surge is impressed, so it requires much fewer reliability than that of the logic element which switches frequently. Therefore, it becomes possible to use lateral polysilicon diodes, which had not been ensured reliability for enduring ON/OFF switching operation to be expected in ten years since it includes a lot of defects due to the polycrystal, as ESD protection element.

The use of the lateral polysilicon diodes as ESD protection element decrease the parasitic capacitances between the diode and Si substrates, i.e. wells, dramatically, thereby preventing high-frequency signal leaking into the Si substrate of low resistance via the parasitic capacitances. As shown in FIG.7, the cross wise length of the lateral polysilicon diodes is determined with the region to form PN junction and the region to form electrodes for P-type and N-type region 85 and 86 (that is, the required region to form a contacts 88 connected to P-type and N-type regions 85 and 86) and it is approximately 5 μm at most. With assuming width of the diode to be 100 μm as same as the above

example of the MOS transistor, it could be thought that a conductor having its area S =500 μm^2 (S=5 μm×100 μm) is counterposed to Si substrate interposing the insulating layer of silicon oxide. With assuming the thickness "d" of the insulating layer to be 0.35 μm, the parasitic capacitances "C" between Si substrate and the conductor, i.e. the lateral polysilicon diodes, is obtained by the equation $C= \varepsilon_{ox} \cdot d/S$ (ε_{ox} is a dielectric constant of insulating layer (SiO_2)), so the capacitance C is 0.05 pF for one diode. The value is reduced to 1/20(0.5 %), compared with 1.02 to 1.22 pF of the parasitic capacitances for MOS transistors in the prior art ESD protection circuit. It means that impedance due to the parasitic capacitances becomes 20 times or more than that of ESD protection element employing with MOS transistor at high-frequency, thereby preventing completely that high-frequency signals are passed through the parasitic capacitances and flow into the Si substrate. Thus, loss of the signal at the low resistance Si substrate shall be decreased dramatically. Accordingly it is achieved a sophisticated and highly reliable high-frequency semiconductor device having high ESD resistance, preventing destruction of Si-MOS transistor in the device without deteriorating high frequency characteristics.

As the parasitic capacitances along with lateral polysilicon diodes, there is depletion layer capacitance 39 and 40 of PN junction in addition to parasitic capacitances 41 and 42 between a Si substrate as shown in equivalent circuit diagram of FIG.9. In a case where PN junction is made by the following methods, the impurity concentration often becomes very high such as approximately 10^{20} cm^{-3}, and depletion layer capacitance becomes relatively high. In a case where lateral polysilicon diodes is used for the prior art semiconductor device, the

total parasitic capacitances, including the depletion layer capacitance, is important. However, as mentioned above, in the high frequency device employing with Si-MOS transistor, in which loss of the high-frequency signals at the low resistance Si substrate (diagrammatically shown as resistances 33 and 34 in FIG.9) shall cause a problem, it is more important to reduce the parasitic capacitances between Si substrate.

Therefore, by employing with clamp circuit using lateral polysilicon diodes as ESD protection circuit, the present invention satisfies the request, raised with the high-frequency semiconductor device employing Si-MOS transistors, to reduce not total parasitic capacitances but the parasitic capacitances between the Si substrate. At the same time, as mentioned above, the present invention is also directed to and solves various problems preventing application of lateral polysilicon diodes in the prior art, and has new important effects and novelty.

As described above, the clamp circuit, which uses the lateral polysilicon diodes as an ESD protection element, is formed only on high-frequency I/O signal line among all I/O lines of the high-frequency device employing with Si-MOS transistor, thereby preventing destruction of Si-MOS transistor without causing mis-operation and deteriorating high frequency characteristics. Therefore a sophisticated and highly reliable high frequency semiconductor device with high ESD resistance is achieved.

[EMBODIMENT 2]

In the present embodiment, as shown in FIG. 10, "m" pieces of lateral polysilicon diodes 38a, 38b, ... , 38m are connected in series

between high-frequency I/O signal line which connects high-frequency signal I/O pad 30a with the internal circuit 100 and VDD (positive voltage supplied externally). The forward direction of these diodes is the direction from the high-frequency I/O signal line to the VDD. Further, "n" pieces of lateral polysilicon diodes 37a, 37b, ... , 37n are connected in series between the ground (GND) and the high-frequency I/O signal line. The forward direction of these diodes is the direction from the GND to the high-frequency I/O signal line.

With representing the voltage of VDD as V_{dd}, the total number (m+n) of lateral polysilicon diodes is desired to meet the following equation (1).

$V_{dd}/(m+n)<1.1[V]$...equation (1)

In the lateral polysilicon diode, PN junction is formed laterally. But practically, as described in later, a "i" region in which few or no impurities are doped is typically formed between "P" and "N" region to improve characteristic of diode. Because of this PIN junction, such a diode is called PIN diode and appears in the article of S. M. Sze, "Physics of Semiconductor Devices pp.117" (hereinafter article 6) for example. When a voltage is applied to the PIN type lateral polysilicon diodes, most of applied voltage is impressed to "i" region of high resistance. When it is assumed that a reverse voltage is impressed, and the impressed voltage to the "i" region becomes larger than band gap voltage of Si (approx.1.1 [V]), energy band shall be shifted larger than the band gap of Si in the "i" region, thereby causing so called "tunnel effect" in which electrons in valence band passes through to conductive band (FIG.11 (b)). This is called "the tunnel effect between bands" as described in the publication entitled "Flash memory technological handbook" from

science forum Inc. (hereinafter article 7). As mentioned above, polysilicon has a lot of defects and large grain size so that deep trap of energy level is formed. Thus, when the tunnel effect between bands are caused, leakage current at reverse bias shall be increased dramatically with encouraging generation of tunnel current via these deep trap of energy levels (refer to the FIG.11(c)).

In the present embodiment, plurality of diodes are connected in series to configure a clamp circuit so that a reverse bias voltage impressed to each diode is less than band gap voltage of Si. Therefore tunnel effect between bands is prevented, thereby reducing DC current consumption with reducing reverse leakage current of the lateral polysilicon diodes. In the prior art, when plural number of diodes are connected in series, required voltage to turn ON the diodes is doubled, tripled, ... , and results in increasing of power consumption. Further, diodes may not be turned ON since the required turn ON voltage becomes higher than the external supply voltage. According to the present invention, only reverse bias is impressed to the diode during ordinary operation of the device, and forward voltage is impressed when ESD is occurred. A surge voltage due to ESD is extremely higher than turn ON voltage of the diodes in series, therefore, the diodes is turned ON to flow current through them so as to protect the internal circuit from ESD. Thus, according to the present invention, it becomes possible to apply series connected diodes for the first time.

As described above, by applying the clamp circuit wherein lateral polysilicon diodes is employed as an ESD protection element only for the high-frequency I/O signal line among all I/O lines of the high-frequency device employing Si-MOS transistor circuit, it becomes

possible to prevent destruction of Si-MOS transistor circuit element due to ESD without causing mis-operation and deteriorating high frequency characteristics. Therefore, a sophisticated and highly reliable high frequency semiconductor device with high ESD resistance is achieved.

The clamp circuit, wherein plurality of diodes are connected in series and therefore only applicable as ESD protection circuit, prevent a tunnel effect between bands when the lateral polysilicon diodes are reversely biased, thereby reducing reverse bias leakage current results in reduction of DC current consumption.

[EMBODIMENT 3]

As for Embodiments 1 and 2, the clamp circuits of lateral polysilicon diode(s) are attached between the VDD and the signal line and between the GND and the signal line. However, the clamp circuit of lateral polysilicon diode(s) may be attached only to either of them, i.e. between the VDD and the signal line or between the GND and the signal line. The clamp circuit of lateral polysilicon diode(s) may be attached to either of them, and the prior art clamp circuit may be attached to another.

[EMBODIMENT 4]

The manufacturing process of the high-frequency semiconductor device of embodiment 1, 2, and 3 are described with referring to FIG. 12, 13, 14, 15, 16, and 17. FIG. 12, 13, 14, 15, 16, and 17 shows manufacturing process of high-frequency semiconductor device in which NMOS transistor, PMOS transistor and lateral polysilicon diodes are formed on region 91 for NMOS, region 92 for

PMOS and region 93 for diode respectively.

First of all, oxide film 2 for separation and insulation is formed on the Si substrate 1, and further, wells are formed at the region 91 and 92 by ion implantation (FIG. 12(a)).

Next, a gate insulating film 3 is formed, and further, a non-doped polysilicon layer 4 is formed (FIG. 12(b)).

Then a resist pattern 51 is formed, and impurity ion is injected into exposed region of the polysilicon layer 4 which is to be a gate electrodes of NMOS transistor as shown by arrow A. (FIG. 12(c)).

The resist pattern 51 is removed, and the polysilicon layer 4 is patterned to leave regions to be gate electrode of NMOS transistor, gate electrode of PMOS transistor and lateral polysilicon diodes with using another resist pattern (not shown) (FIG. 13(a)).

Resist pattern 52 is formed, and as shown by arrow B in the figure, ion implantation is carried out for forming LDD structure at source and drain of NMOS transistor (FIG. 13(b)).

The resist pattern 52 is removed and a resist pattern 53 is formed, and as shown by arrow C, ion implantation is carried out for forming LDD structure at source and drain of PMOS transistor (FIG. 13(c)).

The resist pattern 53 is removed and dielectric film sidewall 5 are formed on the lateral side of the polysilicon layer 4(FIG. 14(a)).

After that, resist pattern 54 is formed, and simultaneously with ion implantation into source and drain of NMOS transistor, ions are injected into a N-type region of the lateral polysilicon diodes as shown by arrow D (FIG.14 (b)).

Resist pattern 54 is removed and another resist pattern 55 is

formed, and simultaneously with ion implantation into source and drain of PMOS transistor, ions are injected into a P-type region of the lateral polysilicon diodes as shown by arrow E (FIG.14 (c)).

Resist pattern 55 is removed and insulating film 6 for preventing SALICIDE (self-aligned silicide) is layered (FIG. 15(a)). Then, resist pattern 56 is formed (FIG. 15(b)), and the insulating film 6 is patterned (FIG. 15(c)) so that the dielectric film 6 on NMOS and PMOS is removed.

Accordingly, silicide wiring 7 is formed on gates, sources and drains of NMOS transistor and PMOS transistor by self-aligned silicide formation.

Hereinafter, interlayer insulating film 8 is layered (FIG. 16(b)), and contact hole 9 for NMOS transistor, PMOS transistor and the lateral polysilicon diodes are formed in the interlayer insulating film 8 (FIG. 17(a)).

A contact 10 of conductive material are formed within the contact hole 9, then metal wiring 11 is formed (FIG. 17(a)).

Hereinafter, processes for depositing interlayer insulating film, forming contact hole and contact (it is generally called "via hole" and "via" in second and succeeding layer) and forming metal wiring are repeated required time, thereby forming metal wiring having required number of layers. By forming passivation film for protection on the metal wiring of the uppermost layer, and then removing the protection film on the I/O pad, finally high frequency semiconductor device is completed.

In the above-mentioned description, ion implantation for source and drain of PMOS and ion implantation for the gate electrode of

PMOS are performed simultaneously. However, the impurity ion implantation for the gate electrodes of PMOS transistor can be carried out immediately after or before injecting impurity ion into the gate electrodes of NMOS transistor (FIG. 12(c)).

[EMBODIMENT 5]

Another example of the manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 are described with referring to FIG. 18, 19, and 20. FIG. 18, 19, and 20 shows the manufacturing process of the high-frequency semiconductor device wherein NMOS transistor, PMOS transistor, and the lateral polysilicon diodes are formed on the region 91 for NMOS, region 92 for PMOS and region 93 for diode respectively.

First of all, the oxide film 2 for separation and insulation is formed on the Si substrate 1, and wells are formed at the region 91 and 92 by ion implantation (FIG. 18(a)).

Next, the gate insulating film 3 is formed, and further non-doped polysilicon layer 4 is formed (FIG. 18(b)).

Then the resist pattern 51a is formed. Simultaneously with impurity ion implantation into exposed region of the polysilicon layer 4 which is to be a gate electrodes of NMOS transistor, ions are injected into a N-type region of the lateral polysilicon diodes as shown by arrow A (FIG. 18(c)).

The resist pattern 51a is removed, and the polysilicon layer 4 is patterned to leave regions to be a gate electrode of NMOS transistor, a gate electrode of PMOS transistor and lateral polysilicon diode with using another resist pattern (not shown) (FIG. 19(a)).

Resist pattern 52a is formed, and as shown by arrow B, ion implantation is carried out for forming LDD structure at source and drain of NMOS transistor (FIG. 19(b)).

The resist pattern 52a is removed and another resist pattern 53a is formed, and as shown by arrow C in the figure, ion implantation is carried out for forming LDD structure at source and drain of PMOS transistor (FIG. 19(c)).

The resist pattern 53a is removed and dielectric film sidewall 5 are formed on the lateral side of the polysilicon layer 4 (FIG. 20(a)).

Resist pattern 54a is formed, ions are injected into source and drain of NMOS transistor as shown by arrow D (FIG. 20(b)).

Further, the resist pattern 54a is removed and another new resist pattern 55a is formed. And simultaneously with ion implantation into source and drain of PMOS transistor, ions are injected into a P-type region of the lateral polysilicon diodes as shown by arrow E (FIG. 20(c)).

Hereinafter, silicide wiring, interlayer insulting film, a metal wiring and a passivation film are formed in the same manner as the embodiment 4.

In the above-mentioned description, ion implantation for source and drain of PMOS transistor and ion implantation for the gate electrodes of PMOS are performed simultaneously. However, the impurity ion implantation for the gate electrodes of PMOS transistor can be carried out immediately after or before injecting impurity ion into the gate electrodes of NMOS transistor (FIG. 18(c)).

[EMBODIMENT 6]

Another manufacturing process of the high-frequency

semiconductor device of embodiment 1, 2, and 3 are described with referring to FIG. 21,22,23 and 24. FIG.21, 22, 23 and 24 show the manufacturing process of the high-frequency semiconductor device wherein NMOS transistor, PMOS transistor, a lateral polysilicon diodes and a capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for diode and region 94 for capacitor respectively.

First of all, the oxide film 2 for separation and insulation is formed on the Si substrate 1, and wells are formed at the region 91 and 92 by ion implantation (FIG. 21(a)).

Further, polysilicon layer 14 in which N-type impurities are doped is formed (FIG. 21(b)).

This polysilicon layer 14 is patterned (FIG. 21(c)) to leave regions to be a lower electrode of the capacitor and a lateral polysilicon diodes.

Hereinafter, an dielectric film 15 for capacitor is laminated and patterned (FIG. 22(a)).

The gate insulating film 3 is formed, and further a non-doped polysilicon layer 24 is formed. Impurity ions are injected through a resist pattern into the polysilicon layer 24 to be a gate electrode of the NMOS transistor. Then the polysilicon layer 24 is patterned using the resist pattern so as to leave regions to be a gate electrode of NMOS transistor, a gate electrode of PMOS transistor and an upper electrode of capacitor (FIG. 22(b)).

A resist pattern 52b is formed, and as shown by arrow B, ion implantation is carried out for forming LDD structure at source and drain of NMOS transistor (FIG. 22(c)).

The resist pattern 52b is removed and another resist pattern

53b is formed, and ion implantation is carried out for forming LDD structure at source and drain of PMOS transistor as shown by arrow C in the figure (FIG. 23(a)).

The resist pattern 53b is removed and dielectric film sidewall 5 are formed on the lateral side of the polysilicon layer 14 and 24 (FIG. 23(b)).

Further, a resist pattern 54b is formed. And, simultaneously with ion implantation into source and drain of NMOS transistor, ions are injected into a N-type region of the lateral polysilicon diodes as shown by arrow D (FIG. 24(a)).

Further, the resist pattern 54b is removed and another new resist pattern 55b is formed. And, simultaneously with ion implantation into source and drain of PMOS transistor, ions are injected into a P-type region of the lateral polysilicon diodes as shown by arrow E (FIG. 24(b)).

Hereinafter, silicide wiring, interlayer dielectric film, a metal wiring and passivation film are formed in the same manner as the embodiment 4.

In the above-mentioned description, ion implantation for source and drain of PMOS transistor and ion implantation for the gate electrode of PMOS transistor are performed simultaneously. However, the impurity ion implantation can be carried out for the gate electrodes of PMOS transistor immediately after or before injecting impurity ion into the gate electrodes of NMOS transistor (FIG. 22(b)).

[EMBODIMENT 7]

Another manufacturing process of the high-frequency

semiconductor device of embodiment 1, 2, and 3 are described with referring to FIG. 25, 26, 27 and 28. FIG.25, 26, 27 and 28 show the manufacturing process of the high-frequency semiconductor device wherein NMOS transistor, PMOS transistor, a lateral polysilicon diodes and a insulating film of the capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for diode and region 94 for capacitor respectively.

First of all, the oxide film 2 for separation and insulation is formed on the Si substrate 1, and wells are formed at the region 91 and 92 by ion implantation (FIG. 25(a)).

Further, polysilicon layer 14 in which N-type impurities are doped is formed (FIG. 25(b)).

Next, this polysilicon layer 14 is patterned to leave regions to be a lower electrode of dielectric film of the capacitor and a lateral polysilicon diodes (FIG. 25(c)).

Hereinafter, an dielectric film 15 for capacitor is laminated and patterned (FIG. 26(a)). At this time, the dielectric film 15 is left on the polysilicon layer 14 also at the place where the PN junction of the lateral polysilicon diode would be formed.

The gate insulating film 3 is formed, and further a non-doped polysilicon layer 24 is formed. Impurity ions are injected through a resist pattern into regions to be a gate electrode of the NMOS transistor. Then the polysilicon layer 24 is patterned using the resist pattern so as to leave regions to be a gate electrode of NMOS transistor, a gate electrode of PMOS and an upper electrode of the capacitor (FIG. 26(b)). At this time, the polysilicon layer 24 is left on the polysilicon layer 14 also at the place where the PN junction of the lateral polysilicon diode

would be formed.

A resist pattern 52c is formed, and ion implantation is carried out for forming LDD structure at source and drain of NMOS transistor as shown by arrow B (FIG. 26(c)).

The resist pattern 52c is removed and another resist pattern 53c is formed, and ion implantation is carried out for forming LDD structure at source and drain of PMOS transistor as shown by arrow C (FIG. 27(a)).

The resist pattern 53c is removed, and dielectric film sidewall 5 are formed on the lateral sides of the polysilicon layers 14 and 24 (FIG. 27(b)).

After that, the resist pattern 54c is formed, and simultaneously with ion implantation into source and drain of NMOS transistor, ions are injected into a N-type region of the lateral polysilicon diodes as shown by arrow D (FIG. 28(a)).

Further, the resist pattern 54c is removed and another new resist pattern 55b is formed, and simultaneously with ion implantation into source and drain of PMOS transistor, ions are injected into a P-type region of the lateral polysilicon diodes as shown by arrow E (FIG. 28(b)).

Hereinafter, silicide wiring, interlayer insulating film, a metal wiring and a passivation film can be formed in the same manner as the embodiment 4.

In the above-mentioned description, ion implantation for source and drain of PMOS transistor and ion implantation for the gate electrode of the PMOS transistor are performed simultaneously. However, the impurity ion implantation for the gate electrodes of PMOS transistor can be carried out immediately after or before injecting

impurity ion into the gate electrodes of NMOS transistor (FIG. 26(b)).

[EMBODIMENT 8]

The method of forming lateral polysilicon diodes in above-mentioned embodiment 4, 5, 6, and 7 will be further described in detail with referring to FIG. 29, 30, 31, and 32.

FIG. 29(a) is a sectional view of the lateral polysilicon diodes, and FIG. 29(b) is a top view of it. Onto an insulating layer 82 of silicon oxide formed on Si substrate 81, a lateral polysilicon diode composed of P++ region 85a heavily doped with P-type impurities and N++ region 86a heavily doped with N-type impurities is formed. The lateral polysilicon diode is connected with metal wirings 89 via contacts 88.

Such a lateral polysilicon diodes are formed by injecting N-type impurity ions heavily into the region 86a masking the region 85a with a resist pattern (e.g., the resist pattern 54 in the embodiment 4), and further injecting P-type impurity ions heavily into the region 85a masking the region 86a with a resist pattern (e.g., the resist pattern 55 in the embodiment 4). Of course, the procedure of ion implantations of N-type and P-type may be changed.

FIG. 30(a) is a sectional view of the lateral polysilicon diodes, and FIG. 30(b) is a top view of it. Onto an insulating layer 82 of silicon oxide formed on Si substrate 81, a lateral polysilicon diode composed of P++ region 85b heavily doped with P-type impurities, N+ region 87b doped with N-type impurities and N++ region 86b heavily doped with N-type impurities is formed. The lateral polysilicon diode is connected with metal wirings 89 via contacts 88.

The lateral polysilicon diode of FIG.30 can be made as follows.

Firstly, entire region of 85b, 87b and 86b are formed from polysilicon doped with N-type impurities. Next, N-type impurity ions are heavily injected into the region 86b masking the region 85b and 87b with a resist pattern, and further P-type impurity ions are heavily injected into the region 85b masking the region 87b and 86b with a resist pattern. Of course, the procedure of ion implantations of N-type and P-type may be changed.

Moreover, according to the embodiment 7, it is possible to define precise boundaries between of the region 87b and the region 86b, and between the region 87b and the region 85b respectively, with using the polysilicon layer 24 and/or the dielectric film 15 formed on the polysilicon layer 14 at the place where the PN junction of the lateral polysilicon diode would be formed (FIG.26 (b)), without using resist pattern. It is possible to keep the width of the region 87b constantly without varying the width due to declination of resist pattern, and reduce variation of diode characteristics. Therefore, it is possible to realize a high-frequency semiconductor device having high reliability.

FIG. 31(a) is a sectional view of the lateral polysilicon diodes, and FIG. 31(b) is a top view of it. Onto the insulating layer 82 of silicon oxide formed on the Si substrate 81, a lateral polysilicon diode composed of P++ region 85c heavily doped with P-type impurities, a region 87c substantially non-doped and N++ region 86c heavily doped with N-type impurities is formed. The lateral polysilicon diode is connected with metal wirings 89 via contacts 88.

The lateral polysilicon diode of FIG.31 can be made as follows. Firstly, entire region of 85c, 87c and 86c are formed from non-doped polysilicon. Next, N-type impurity ions heavily injected into the region

86c masking the region 85c and 87c with a resist pattern, and further P-type impurity ions are heavily injected into the region 85c masking the region 87c and 86c with a resist pattern. Of course, the procedure of ion implantations of N-type and P-type may be changed.

Moreover, according to the embodiment 7, it is possible to define precise boundaries between of the region 87c and the region 86c, and between the region 87c and the region 85c respectively, with using the polysilicon layer 24 and/or the dielectric film 15 on the polysilicon layer 14 to be the lateral polysilicon diodes, without using resist pattern. It is possible to keep the width of the region 87c constantly without varying the width due to declination of resist pattern, and reduce variation of diode characteristics. Therefore, it is possible to realize a high-frequency semiconductor device having high reliability.

FIG. 32(a) is a sectional view of the lateral polysilicon diodes, and FIG. 32(b) is a top view of it. Onto the insulating layer 82 of silicon oxide formed on the Si substrate 81, a lateral polysilicon diode composed of P++ region 85d heavily doped with P-type impurities, a region 87d heavily doped with P-type and N-type impurities and N++ region 86d heavily doped with N-type impurities is formed. The lateral polysilicon diode is connected with the metal wirings 89 via the contacts 88.

The lateral polysilicon diode is formed by injecting N-type impurity ions heavily into the region 87d and 86d masking the region 85d with a resist pattern, further by injecting P-type impurity ions heavily into the region 85d and 87d masking the region 86d with a resist pattern. An impurity concentration of the region 87d is determined by the differences of the concentration between injected N-type impurity ion and P-type impurity ion. Of course, the procedure of ion implantations

of N-type and P-type may be changed.

[EMBODIMENT 9]

As explained so far, in the present invention, the lateral polysilicon diodes 38 and 37 are formed and connected between the high-frequency I/O signal line and the external power supply VDD and/or between the high-frequency I/O signal line and the ground GND so as to prevent destruction of the internal circuit 100 due to ESD with dispersing positive high voltage ESD surge to the external power supply VDD, and negative high voltage ESD surge to the ground GND respectively.

Further, as shown in FIG.33, it is assumed that the case where a protection circuit employing with MOS transistors is attached between the external power supply VDD and the ground GND in the high-frequency semiconductor device having ESD protection circuit employing lateral polysilicon diodes.

In FIG. 33, gate, source and P-well of NMOS transistor 46 are grounded to GND, and its drain is connected to the drain of PMOS transistor 47. On the other hand, gate, source and N-well of PMOS 47 are connected to the external power supply VDD.

A positive high voltage ESD surge impressed to the high-frequency signal I/O pad 30a is dispersed to the VDD through the lateral polysilicon diode 38. The positive voltage surge entered into the VDD is impressed to the source of PMOS 47 being in OFF state, and PN junction of the source diffusion layer thereof causes breakdown, therefore "parasitic bipolar transistor action" is occurred and the current flows into the GND.

At this time, the potential of VDD and the high-frequency I/O signal line rises to the breakdown voltage of PN junction of the source diffusion layer in PMOS 47. Therefore, a reverse high voltage, which equals to the breakdown voltage of PN junction of silicon, is impressed to the lateral polysilicon diodes 37 attached between the high-frequency I/O signal line and GND. Similarly, in a case where a negative high voltage ESD surge is entered into the high-frequency signal I/O pad 30a, the reverse voltage is impressed to the lateral polysilicon diodes 38.

The lateral polysilicon diode is made from polysilicon which includes a lot of defects and traps of deep energy, thereby characteristics thereof is easily deteriorated in case of breakdown due to reverse high voltage. Therefore, it is impossible to protect the circuit against the next ESD surge.

Therefore, in the present embodiment, as shown in FIG.34, a clamp circuit 48, which starts operating at lower voltage than reverse breakdown voltage of the lateral polysilicon diode, is attached between the external power supply VDD and the ground GND.

The positive high voltage ESD surge 45a entered into the VDD shall be dispersed to the GND through the clamp circuit 48 which is turned ON by a slight increase of the potential of the VDD (FIG. 34(b)). Since a turn ON voltage of the clamp circuit 48 is smaller than reverse breakdown voltage of the lateral polysilicon diodes 37, a voltage of VDD shall not become higher. Therefore, a voltage of the high-frequency I/O signal line is kept below the absolute value of the reverse breakdown voltage of the lateral polysilicon diode 37, thereby preventing reverse breakdown of the diode 37 and deterioration of the diode 37 due to the reverse breakdown.

In case of dispersing negative high voltage surge 45b entered into the high-frequency signal I/O pad 30a to the GND through the lateral polysilicon diodes 37, it is also possible to prevent deterioration of the lateral polysilicon diode 38 with preventing reverse breakdown of the diode 38 similarly (FIG. 34(c)).

As described above, according to the present embodiment, it is possible to protect the internal circuit against multiple impressions of ESD surge with preventing deterioration of the lateral polysilicon diode with preventing reverse breakdown thereof.

The embodiment of the clamp circuit 48 will be described with referring to FIG. 35 and 36.

In FIG. 35, the clamp circuit 48 comprises ESD detection circuit 75, inverter 76 and NMOS transistor 77. An output of the ESD detection circuit 75 is connected to the inverter 76, and the output of the inverter 76 is connected to the gate of NMOS 77. NMOS 77 has wide gate so as to allow a large current.

The detection circuit 75 immediately detects sudden increase of VDD voltage due to the impression of ESD surge, and NMOS 77 is turned ON via the inverter 76. Therefore it is possible to disperse a large current from VDD to GND through the NMOS 77.

Accordingly, the voltage of VDD as well as high-frequency I/O signal line shall not increase, thereby preventing that a high voltage larger than reverse breakdown voltage shall be impressed to the lateral polysilicon diodes 37 which is attached between the high-frequency I/O signal line and GND.

In FIG. 36, the clamp circuit 48 comprises "x" pieces of diode 78 attached in series, and forward direction of the diodes is the direction

from the VDD to the GND, thereby enables to flow the large current from VDD to GND when the potential difference between VDD and GND becomes "x" times of the turn ON voltage of the diode 78.

By choosing "x" so that "x" times of the turn ON voltage of the diode 78 should be smaller than the reverse breakdown voltage of the lateral polysilicon diode, the voltage of VDD and the high-frequency I/O signal line can be kept lower than the reverse breakdown voltage of the lateral polysilicon diodes, so that the characteristic of the lateral polysilicon diodes shall not be deteriorated.

In addition to the lateral polysilicon diodes, made of typical PN junction diodes can also be used as the diode 78.

[Effect of the Invention]

According to the present invention, a clamp circuit employing lateral polysilicon diodes as ESD protection element is attached to the high-frequency I/O signal line among all I/O lines of high-frequency device employing Si-MOS transistor so as to decrease the parasitic capacitances between the diode and Si substrate, thereby preventing high-frequency signal leaking into the Si substrate via the parasitic capacitances. Therefore it is possible to achieve sophisticated and highly reliable high frequency semiconductor device.

A DC bias voltage of high-frequency I/O signal line can be set between VDD and GND, thereby keeping the voltage of the signal line lower than that of VDD to prevent the diode being turned ON even if VDD varies. Therefore a sophisticated and highly reliable high frequency semiconductor device with high ESD resistance can be achieved.

Further, the clamp circuit employing lateral polysilicon diodes as ESD protection element is attached to the high-frequency I/O

signal line among all I/O lines of high-frequency semiconductor device employing Si-MOS transistor. The high-frequency I/O signal line shall not cause mis-operation even if a large reverse bias leakage current flows through the lateral polysilicon diodes, since the signal line only supplies bias voltage at DC circuit operation. Therefore, the problem in caused by the large reverse bias leakage current of the lateral polysilicon diodes is solved, and a sophisticated and highly reliable high frequency semiconductor device with high ESD resistance is achieved employing the lateral polysilicon diodes as ESD protection element in the clamp circuit.

Moreover, the lateral polysilicon diodes of the clamp circuit operate only when ESD surge is impressed. Therefore, it is possible to use lateral polysilicon diodes, which had not been ensured reliability for ON/OFF switching operation to be expected in ten years in logic devices as the ESD protection elements.

Plurality of diodes are connected in series to configure the clamp circuit, thereby keeping a reverse bias voltage to be impressed to each diodes less than band gap voltage of Si (approx.1.1 [V]). Therefore tunnel effect between bands is prevented, and thereby reducing DC current consumption with reducing reverse leakage current of the lateral polysilicon diodes.

A high-frequency semiconductor device employing with lateral polysilicon diodes as ESD protection element wherein lateral polysilicon diodes are formed from polysilicon layer for forming lower electrodes of the capacitor, and gate electrodes of MOS transistor are formed from another polysilicon layer. Therefore, it becomes possible to optimize forming condition such as thickness and impurities

concentration and the like of polysilicon layers suitable for the MOS transistor and the lateral polysilicon diodes respectively and high reliability thereof can be realized simultaneously.

By leaving the dielectric film to form the capacitor and/or polysilicon layer to form the upper electrode of the capacitor on PN junction of the lateral polysilicon diodes, it becomes possible to reduce variation of diode characteristics due to declination of resist pattern, and realize a high-frequency semiconductor device having high reliability.

In addition, the "i" region can be formed at the PN junction of the lateral polysilicon diode by leaving the dielectric film to form the capacitor and/or polysilicon layer to form the upper electrode of the capacitor on PN junction of the lateral polysilicon diodes and blocking ion implantation with the film and/or the layer. Moreover, it becomes possible to keep the width of the "i" region of the PIN junction constantly without varying the width due to declination of resist pattern so that the diodes having good and uniform qualities are obtained.

Further, the clamp circuit, which starts operating at lower voltage than reverse breakdown voltage of the lateral polysilicon diodes, is attached between the external power supply VDD and the ground GND. Therefore reverse voltage breakdown of the lateral polysilicon diodes are prevented to avoid deterioration of their characteristics so that it becomes possible to protect the interval circuit against multiple impression of ESD surge.

While there has been described what is at present considered to be preferred embodiment of the invention, it will be understood that various modifications may be made therein, and it is intended to cover in the appended claims all such modifications as fall within the true spirit

and scope of the invention.

[Brief Description of the Drawings]

[FIG. 1] A figure showing a current wave form of ESD (Electro Static Discharge);

[FIG. 2] The circuit diagram illustrating ESD protection circuit employing MOS transistor in OFF state;

[FIG. 3] A figure describing parasitic bipolar transistor action of MOS transistors;

[FIG. 4] A figure illustrating the distance between the gate and the contact of the MOS transistor;

[FIG. 5] An equivalent circuit diagram describing outflow of high-frequency signal through the capacitor of the drain diffusion layer of the MOS transistor;

[FIG. 6] A circuit diagram showing the ESD protection circuit according to the present invention;

[FIG. 7] (a) is a sectional view of the lateral polysilicon diode, and (b) is a top view of it;

[FIG. 8] A figure showing voltage current characteristic of the lateral polysilicon diodes;

[FIG. 9] A figure showing the equivalent circuit describing outflow of the high-frequency signal through the parasitic capacitance for Si substrate and through the depletion layer capacity;

[FIG. 10] A figure showing ESD protection circuit according to the present embodiment;

[FIG. 11] A figure showing the influence of the presence of traps of deep energy in the tunnel effect between bands;

[FIG. 12] A figure showing the manufacturing process of the

high-frequency semiconductor device according to the present invention;

[FIG. 13] A figure showing the manufacturing process following the FIG. 12;

[FIG. 14] A figure showing the manufacturing process following the FIG. 13;

[FIG. 15] A figure showing the manufacturing following the FIG. 14;

[FIG. 16] A figure showing the manufacturing process following the FIG. 15;

[FIG. 17] A figure showing the manufacturing process following the FIG. 16;

[FIG. 18] A figure showing other manufacturing process of the high-frequency semiconductor device according to the present invention;

[FIG. 19] A figure showing the manufacturing process following the FIG. 18;

[FIG. 20] A figure showing the manufacturing process following the FIG. 19;

[FIG. 21] A figure showing further still other manufacturing process of the high-frequency semiconductor device according to the present invention;

[FIG. 22] A figure showing the manufacturing process following the FIG. 21;

[FIG. 23] A figure showing the manufacturing process following the FIG. 22;

[FIG. 24] A figure showing the manufacturing process

following the FIG. 23;

[FIG. 25] A figure showing further still other manufacturing process of the high-frequency semiconductor device according to the present invention;

[FIG. 26] A figure showing the manufacturing process following the FIG. 25;

[FIG. 27] A figure showing the manufacturing process following the FIG. 26;

[FIG. 28] A figure showing the manufacturing process following with the FIG. 27;

[FIG. 29] A figure showing an example of PN junction of lateral polysilicon diodes;

[FIG. 30] A figure showing other example of PN junction of lateral polysilicon diodes;

[FIG. 31] A figure showing still other example of PN junction of lateral polysilicon diodes;

[FIG. 32] A figure showing further still other example of PN junction of lateral polysilicon diodes;

[FIG. 33] A figure showing a protection circuit employing MOS transistor connected between VDD and GND;

[FIG. 34] A figure showing a clamp circuit connected between VDD and GND according to the present invention;

[FIG. 35] A figure showing an example of a clamp circuit connected between VDD and GND;

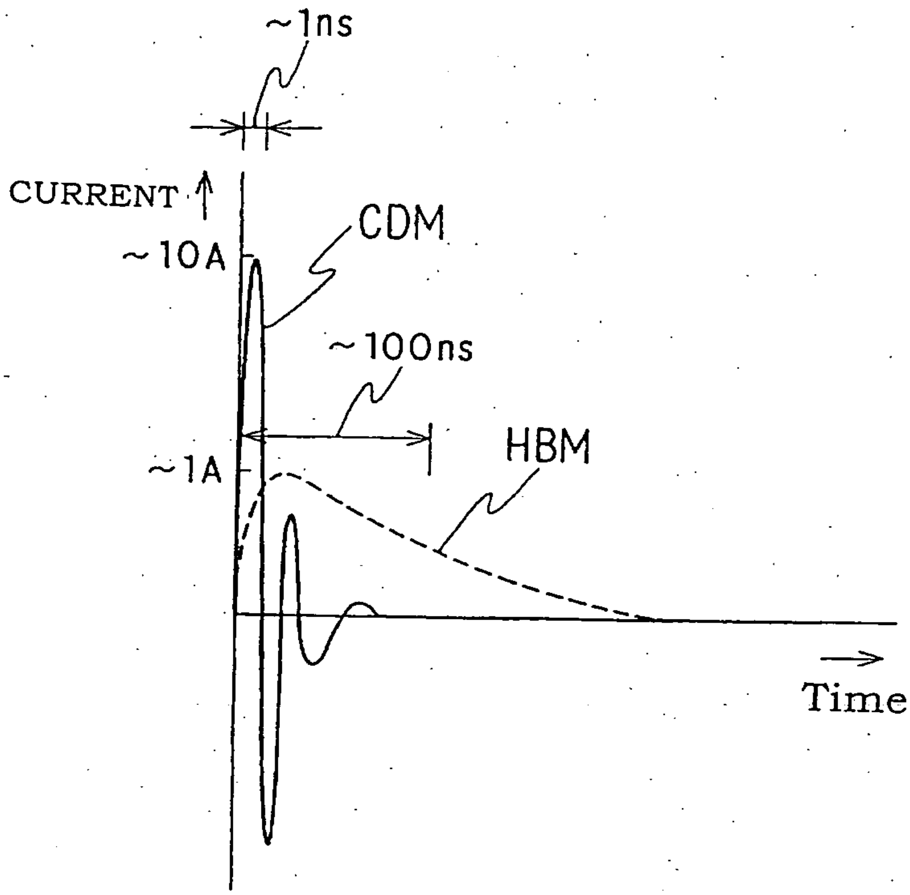
[FIG. 36] A figure showing other example of a clamp circuit connected between VDD and GND.

[Explanation of Reference Numerals]

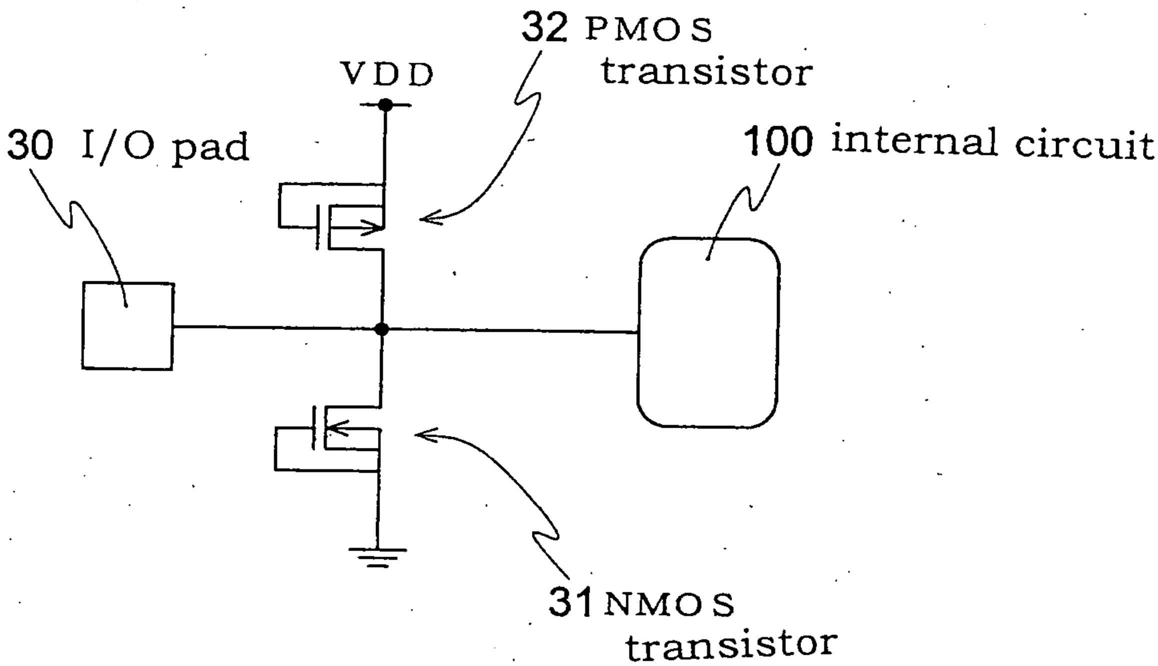
1 Si substrate, 2 oxide film for separation 3, gate insulating film, 4 polysilicon layer (Impurity non-doped), 5 dielectric film sidewall, 6 insulating film for preventing SALICIDE, 7 silicide wiring, 8 interlayer insulating film, 9 contact hole, 10 contact, 11 metal wiring, 14 polysilicon layer (N-type impurity doped), 15 inter-polysilicon dielectric film, 24 polysilicon layer (impurity non-doped), 30 I/O pad, 31 NMOS transistor, 32 PMOS transistor, 37 lateral polysilicon diode, 38 lateral polysilicon diode, 45 surge, 46 NMOS transistor, 47 PMOS transistor, 48 clamp circuit attached between VDD/GND, 51 resist pattern, 52 resist pattern, 53 resist pattern, 54 resist pattern, 55 resist pattern, 56 resist pattern, 75 ESD detection circuit, 76 inverter, 77 NMOS transistor, 78 diode, 82 insulating layer of silicon oxide, 83 interlayer insulating film, 100 internal circuit

[Document Name] DRAWINGS

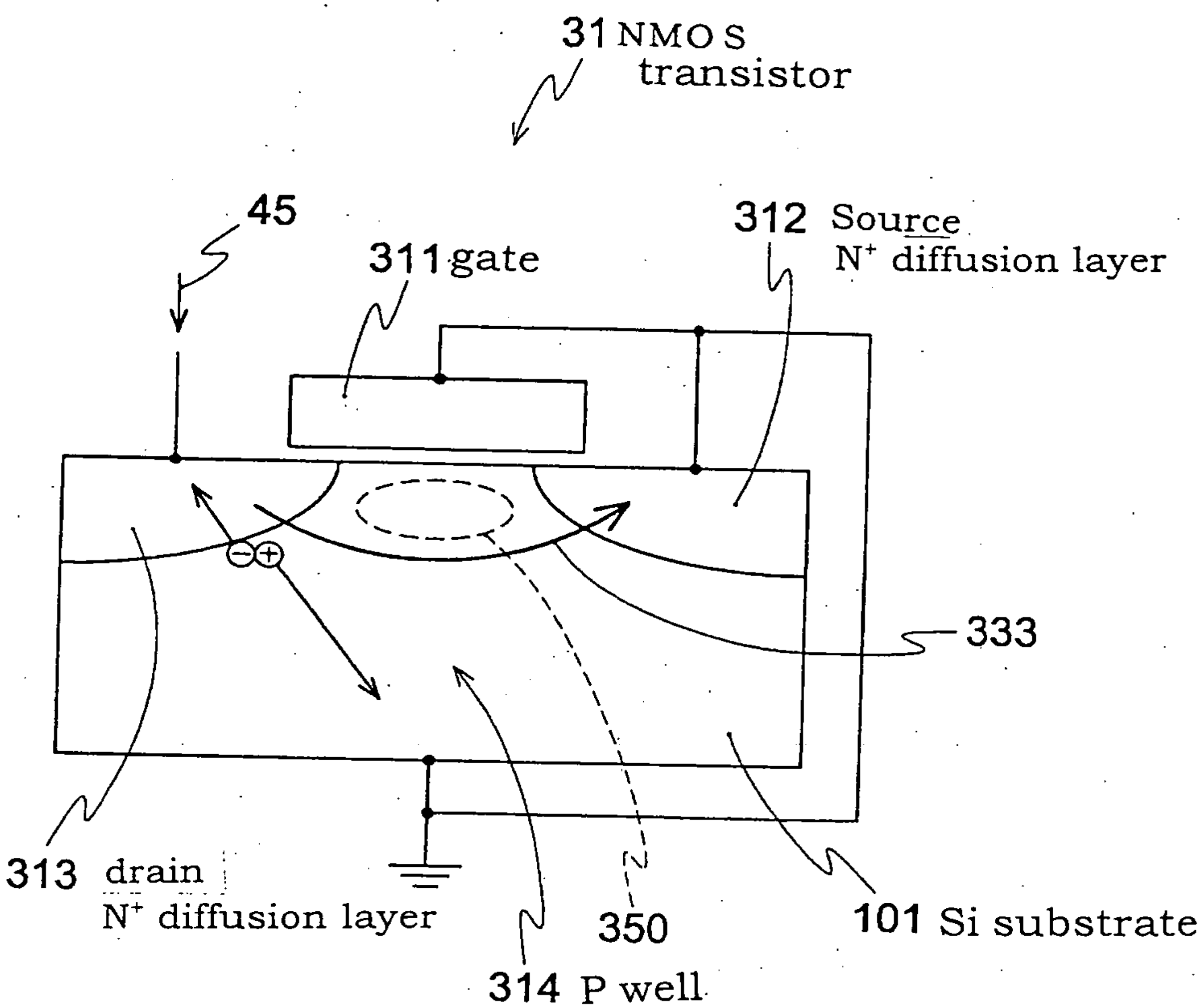
[Fig. 1]



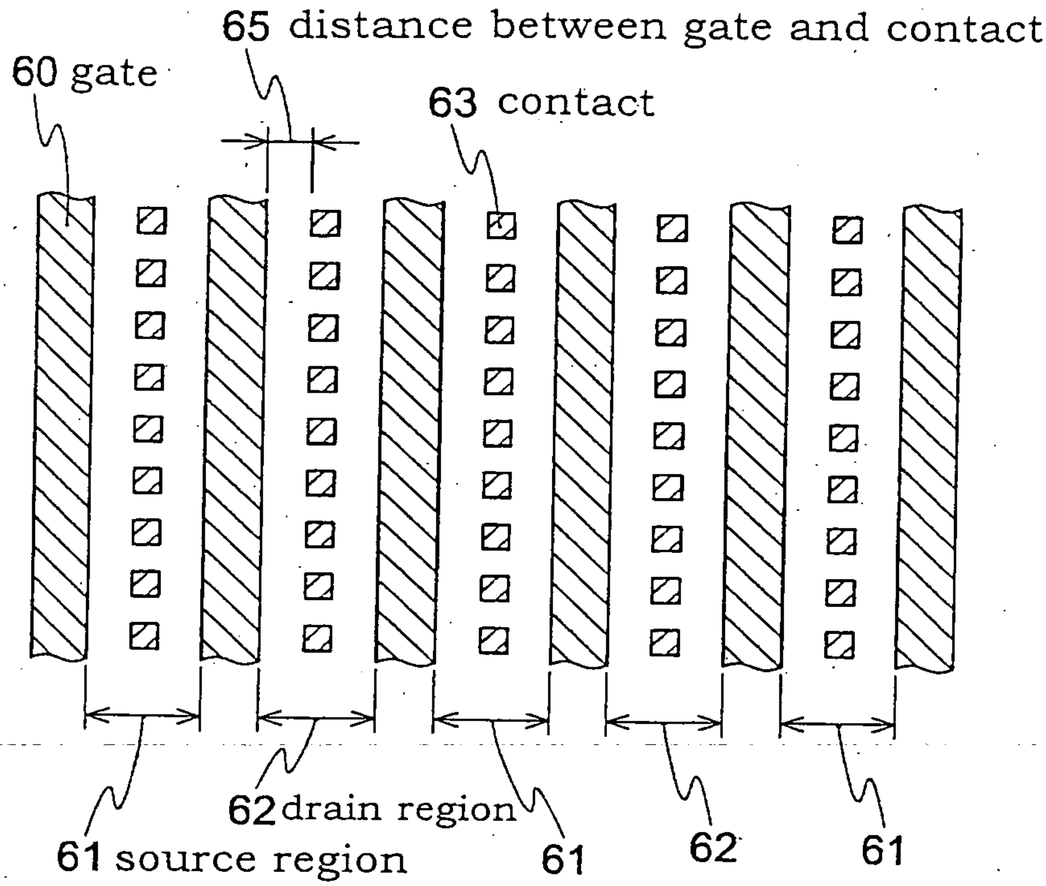
[Fig. 2]


32 PMOS transistor
VDD
30 I/O pad
100 internal circuit
31 NMOS transistor

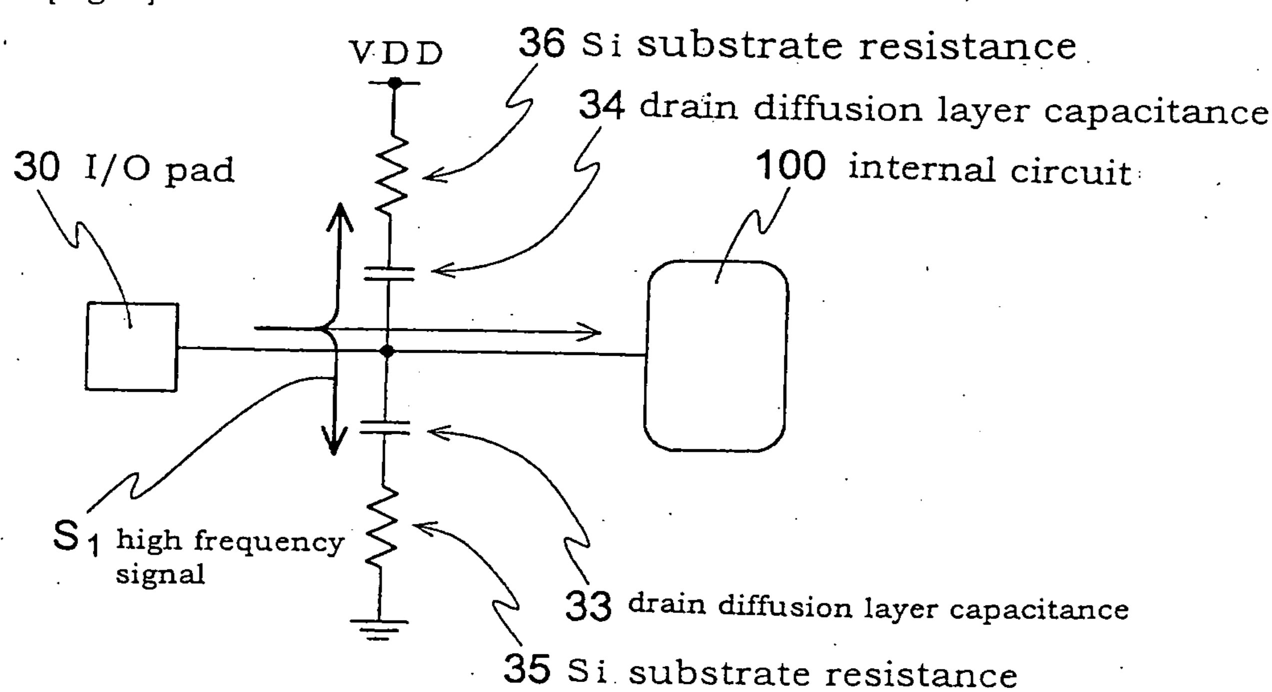
[Fig. 3]


31 NMOS transistor
45
311 gate
312 Source N+ diffusion layer
333
313 drain N+ diffusion layer
314 P well
350
101 Si substrate

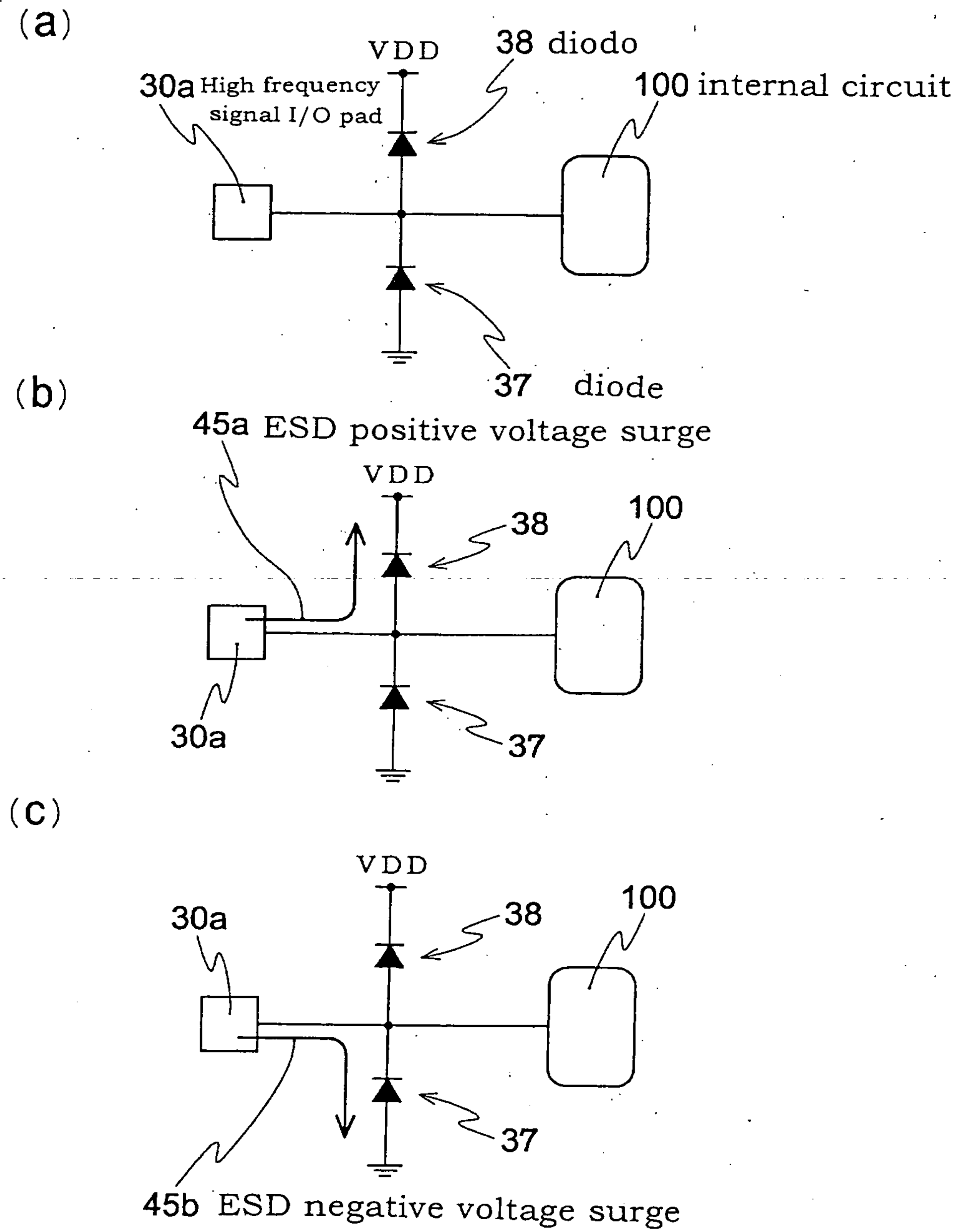
[Fig. 4]


65 distance between gate and contact
60 gate
63 contact
62 drain region
61 source region
61
62
61

[Fig. 5]

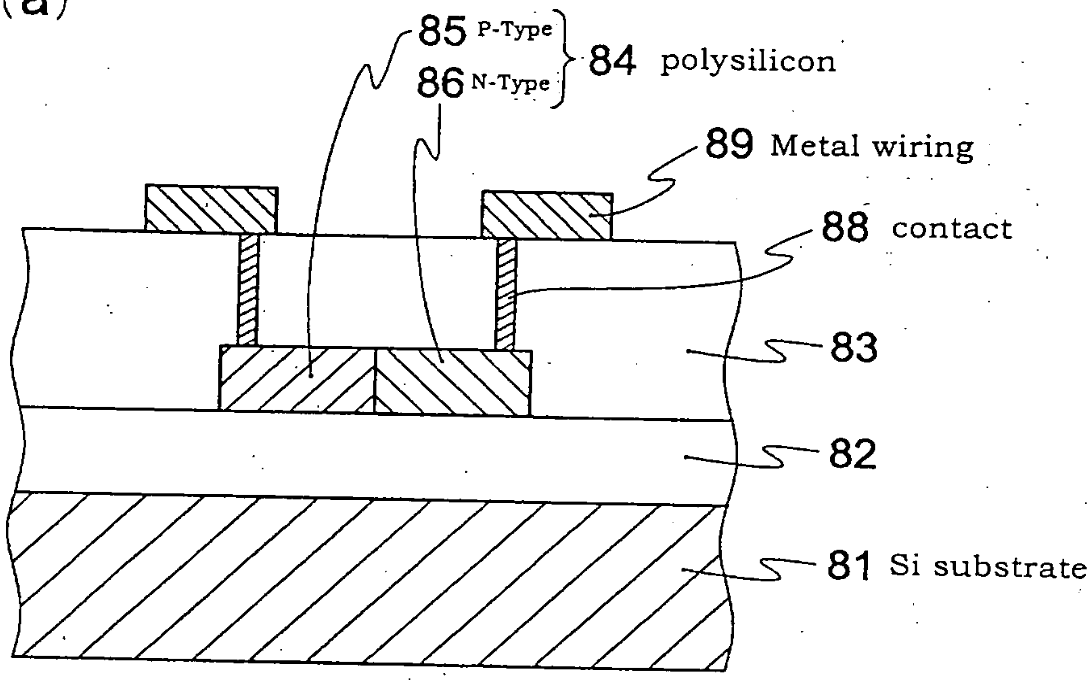

VDD
36 Si substrate resistance
34 drain diffusion layer capacitance
30 I/O pad
100 internal circuit
S1 high frequency signal
33 drain diffusion layer capacitance
35 Si substrate resistance

[Fig. 6]

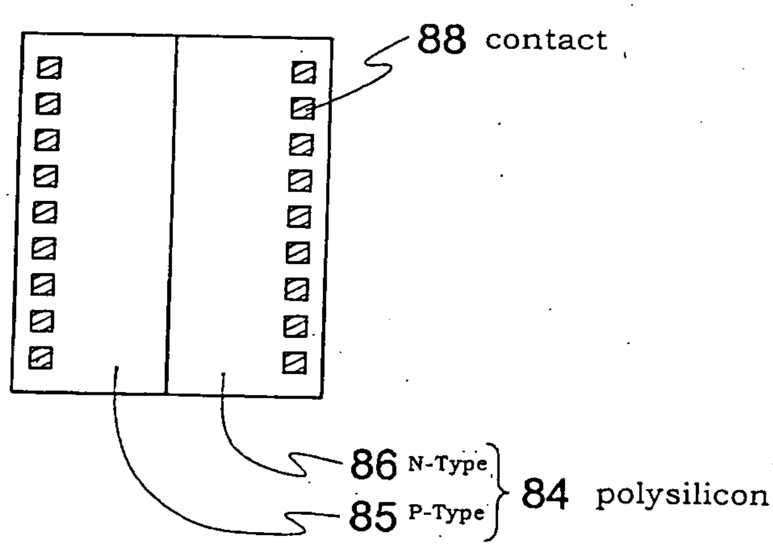

(a)
VDD
38 diodo
30a High frequency signal I/O pad
100 internal circuit
37 diode
(b)
45a ESD positive voltage surge
VDD
38
100
30a
37
(c)
VDD
30a
38
100
37
45b ESD negative voltage surge

[Fig. 7]

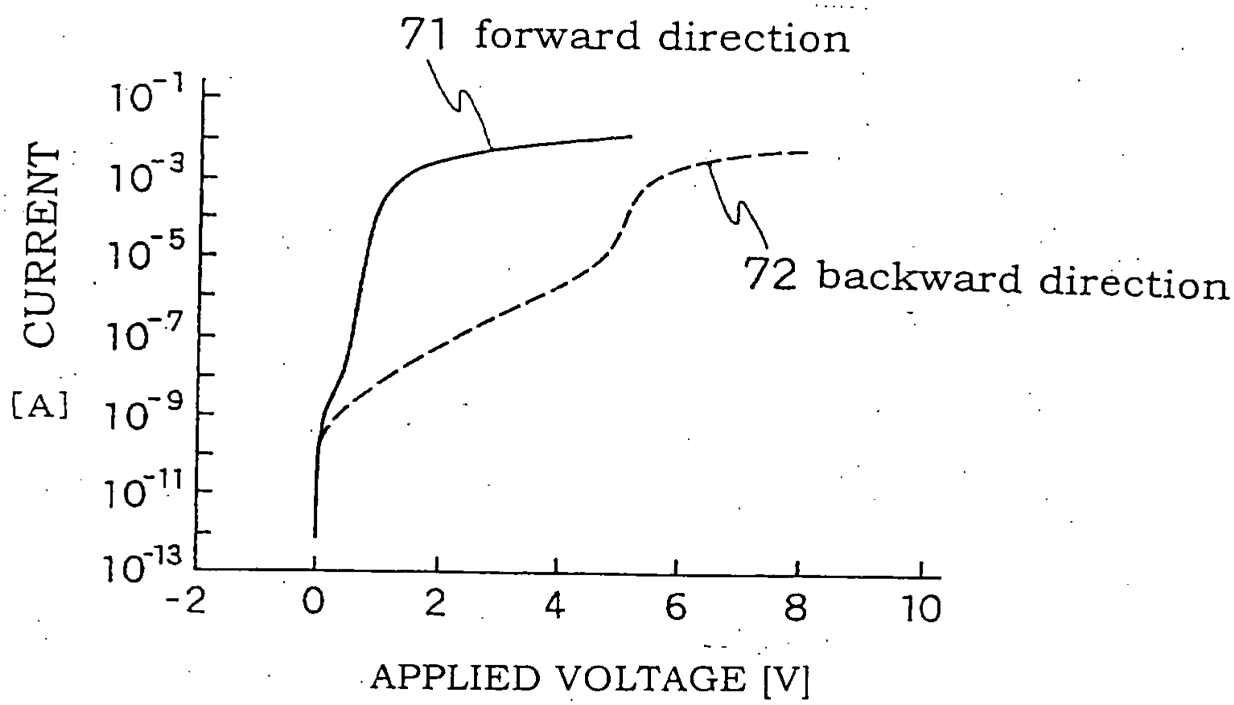
(a)


85 P-Type
86 N-Type
84 polysilicon
89 Metal wiring
88 contact
83
82
81 Si substrate

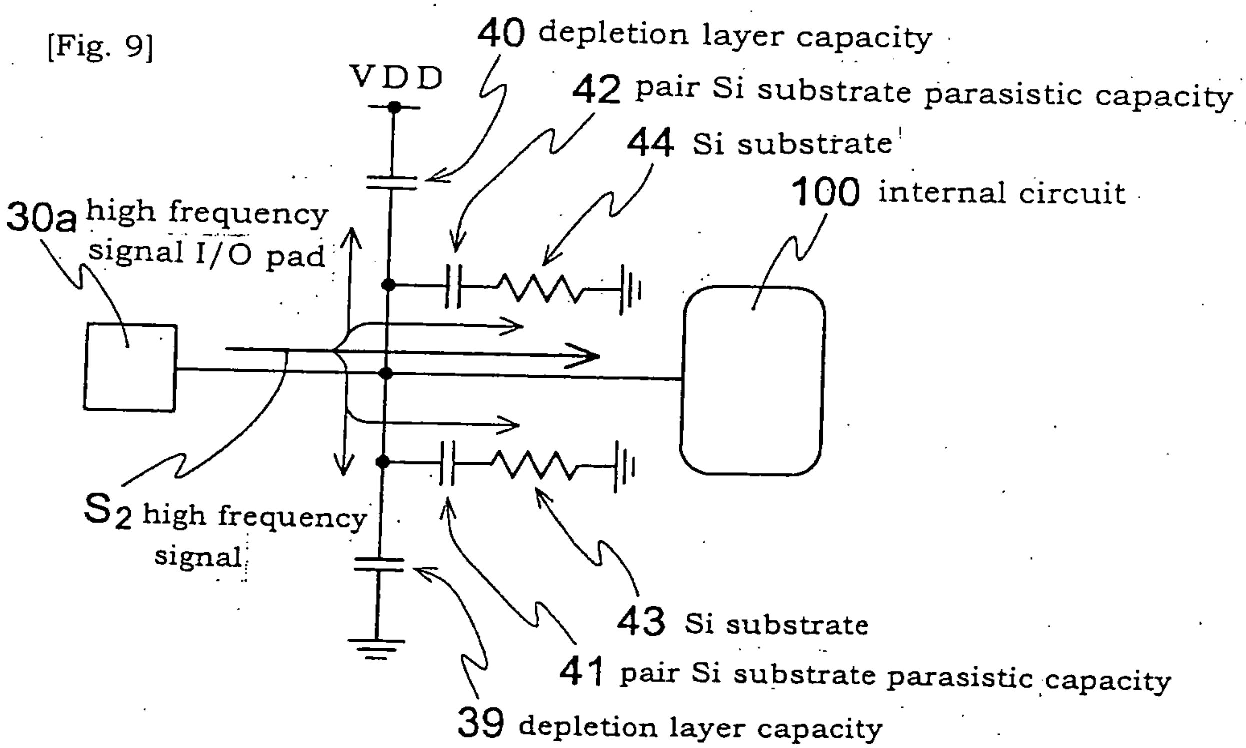
(b)


88 contact
86 N-Type
85 P-Type
84 polysilicon

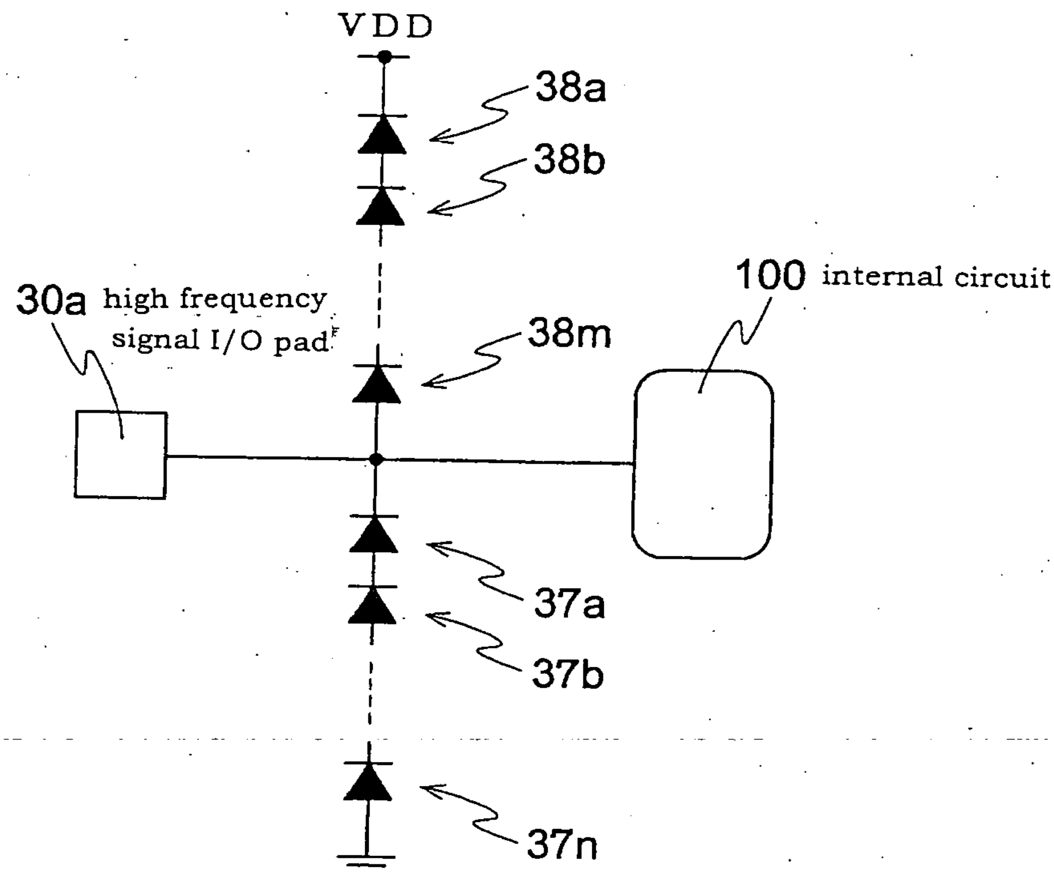
[Fig. 8]


71 forward direction
72 backward direction
CURRENT [A]
10^{-1}
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-2
0
2
4
6
8
10
APPLIED VOLTAGE [V]

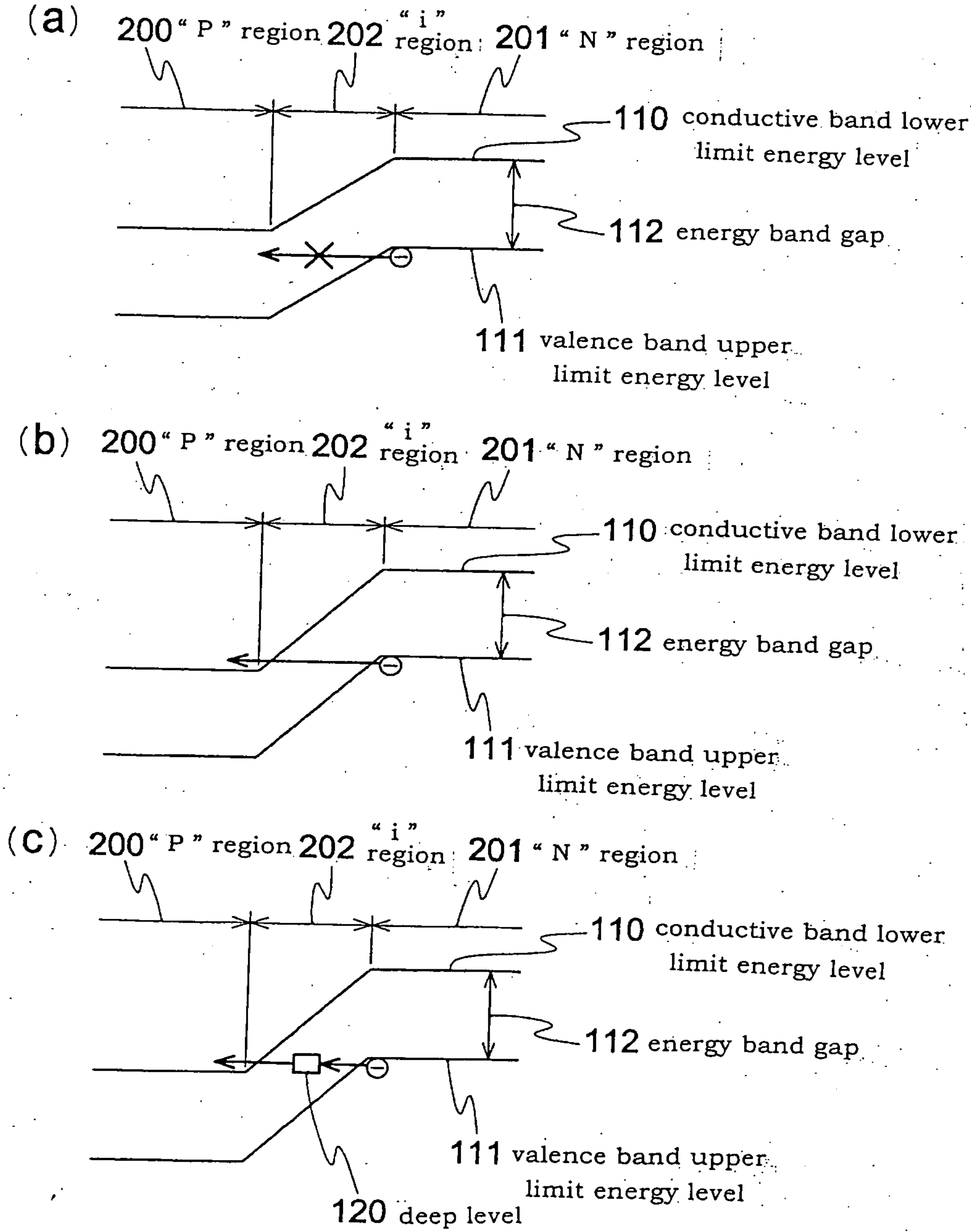
[Fig. 9]


40 depletion layer capacity
VDD
42 pair Si substrate parasistic capacity
44 Si substrate
100 internal circuit
30a high frequency signal I/O pad
S2 high frequency signal
43 Si substrate
41 pair Si substrate parasistic capacity
39 depletion layer capacity

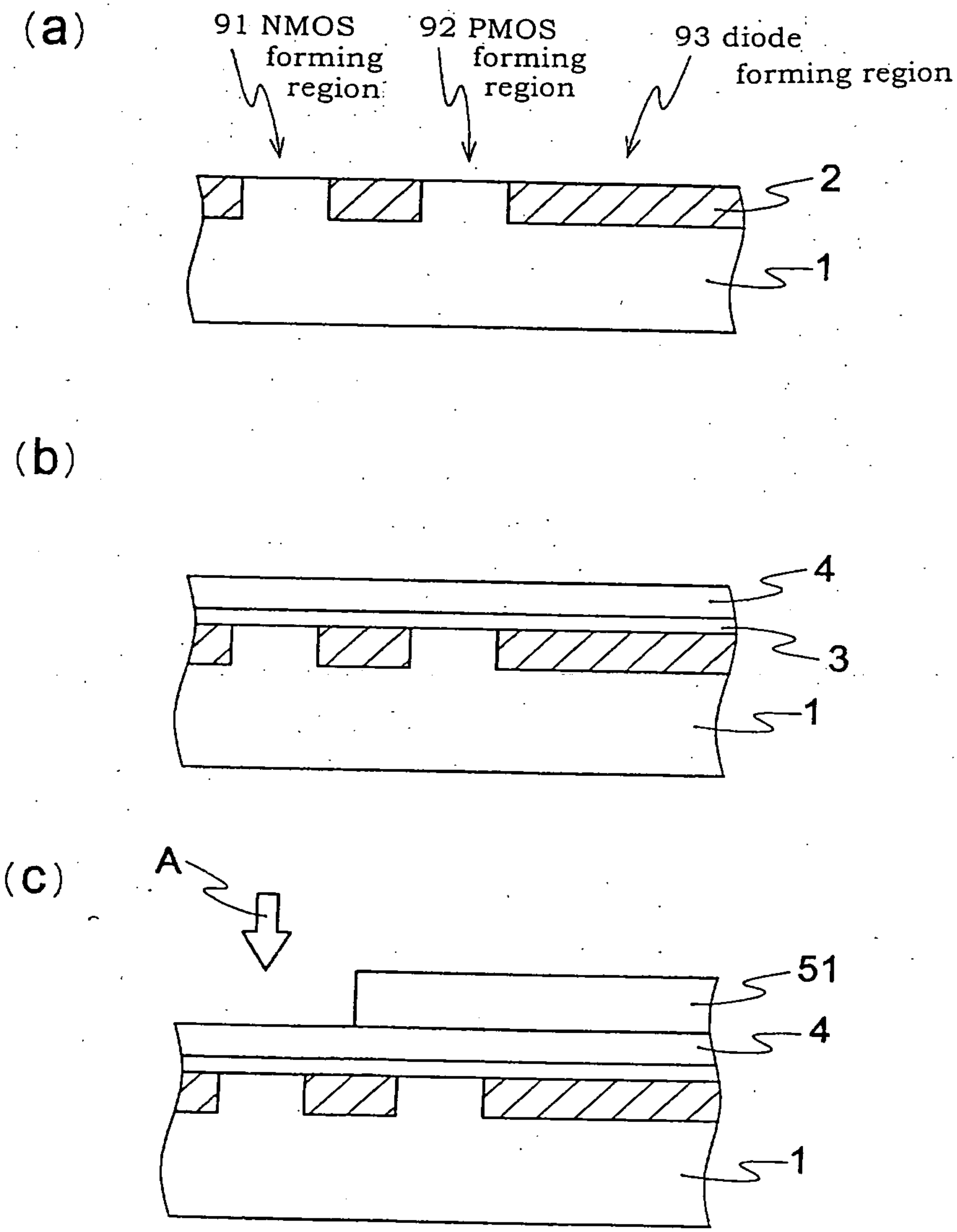
[Fig. 10]


VDD
38a
38b
38m
30a high frequency signal I/O pad
100 internal circuit
37a
37b
37n

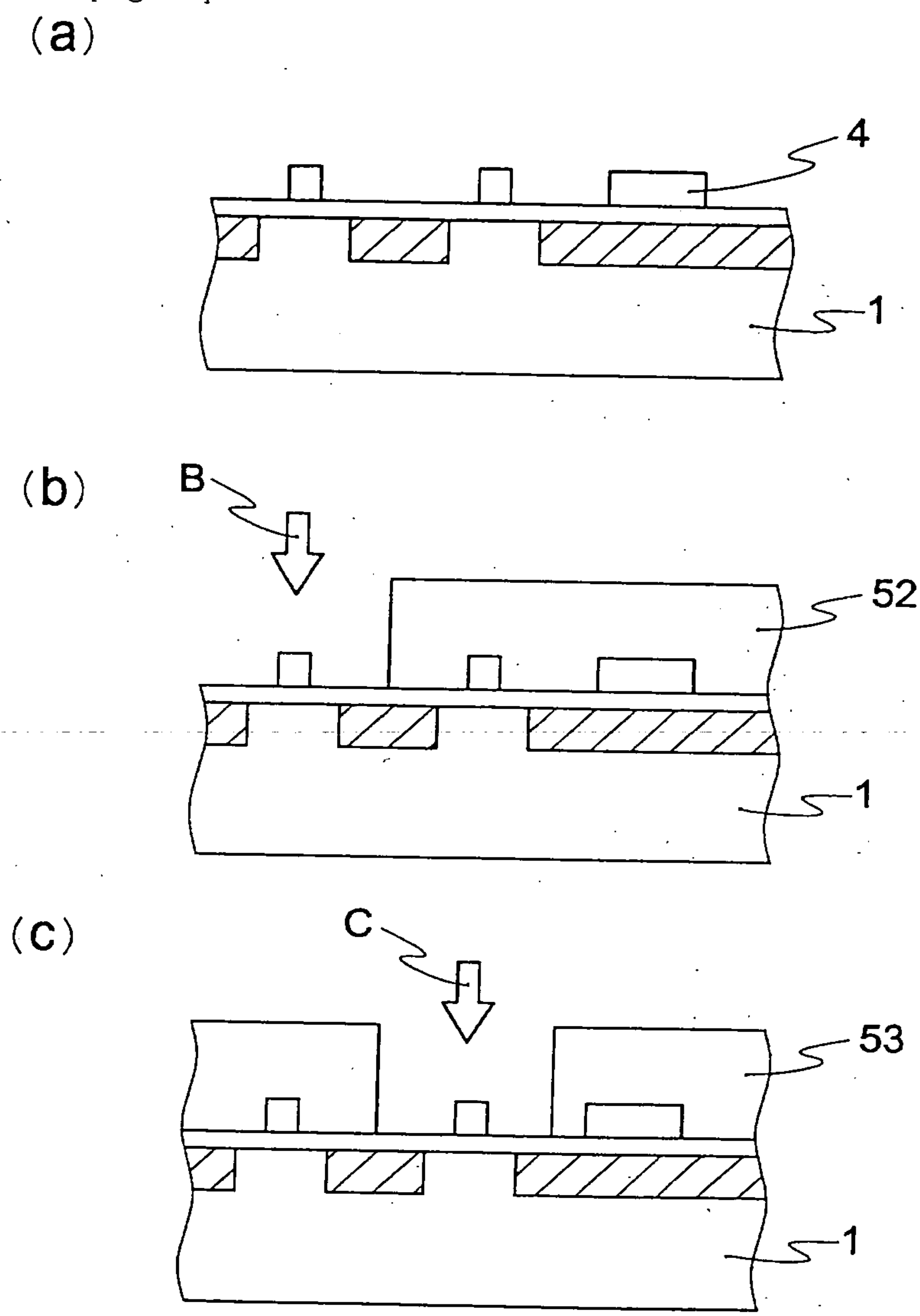
[Fig. 11]


(a)
200 " P " region
202 " i " region
201 " N " region
110 conductive band lower limit energy level
112 energy band gap
111 valence band upper limit energy level
(b)
200 " P " region
202 " i " region
201 " N " region
110 conductive band lower limit energy level
112 energy band gap
111 valence band upper limit energy level
(c)
200 " P " region
202 " i " region
201 " N " region
110 conductive band lower limit energy level
112 energy band gap
111 valence band upper limit energy level
120 deep level

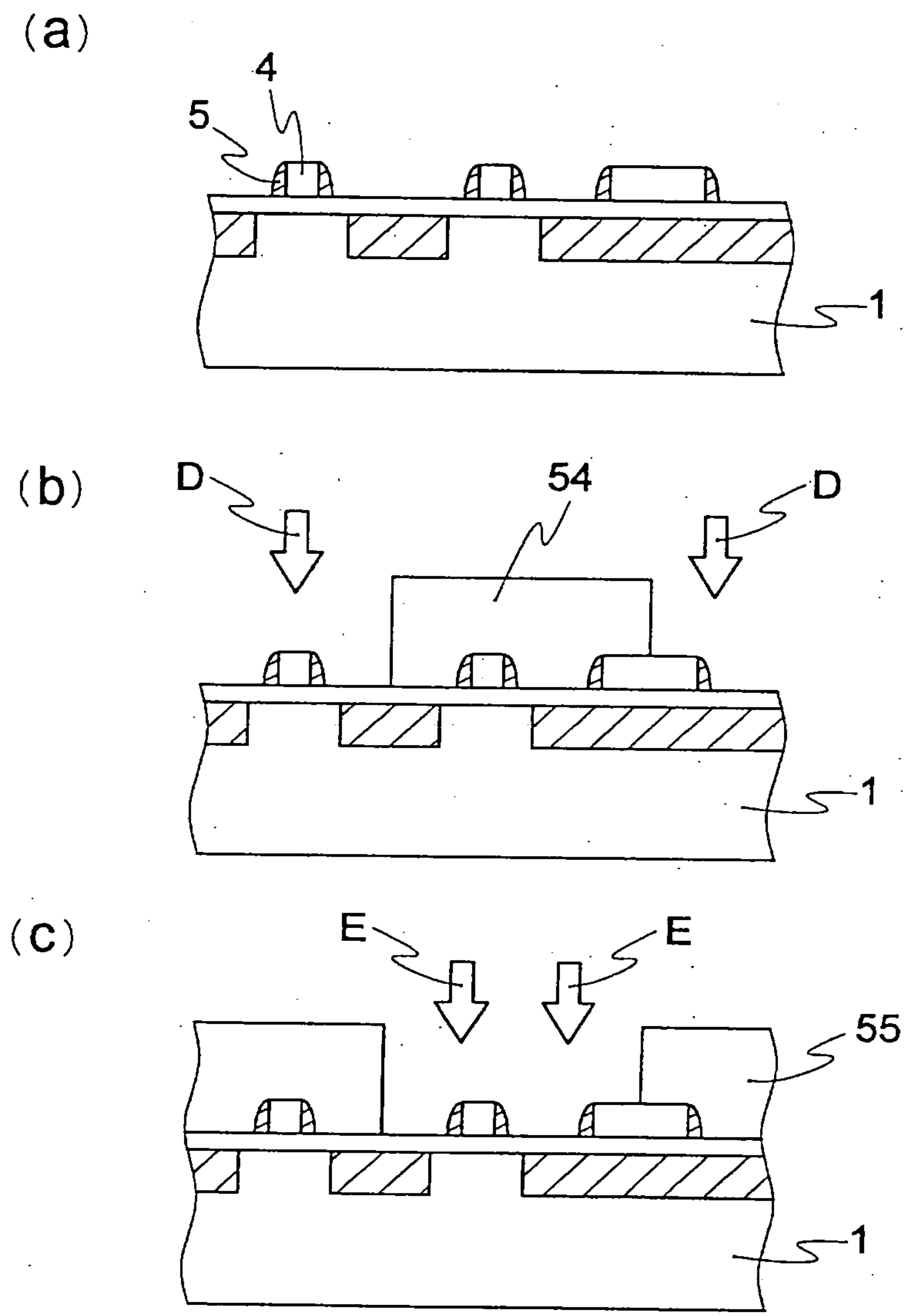
[Fig. 12]


(a)
91 NMOS forming region
92 PMOS forming region
93 diode forming region
2
1
(b)
4
3
1
(c)
A
51
4
1

[Fig. 13]

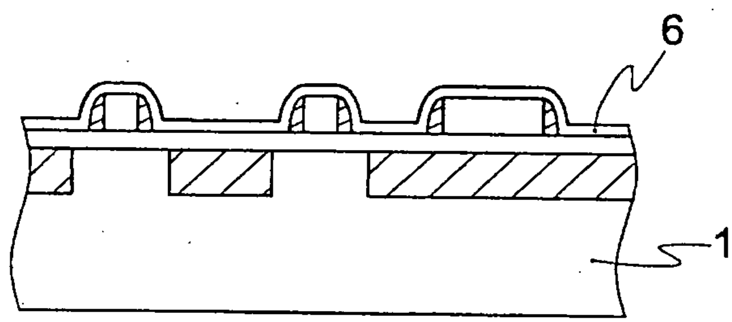


[Fig. 14]

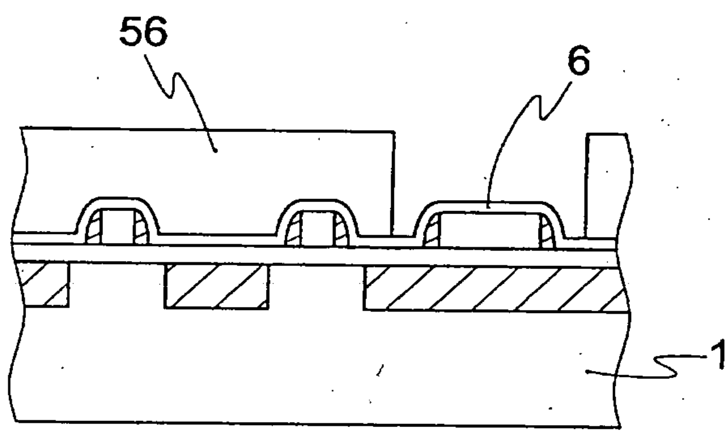


[Fig. 15]

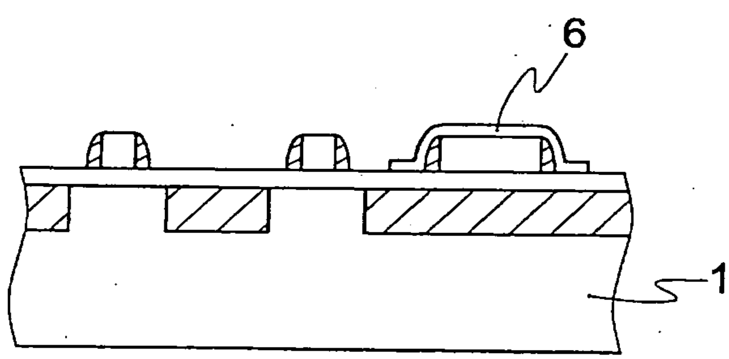
(a)



(b)

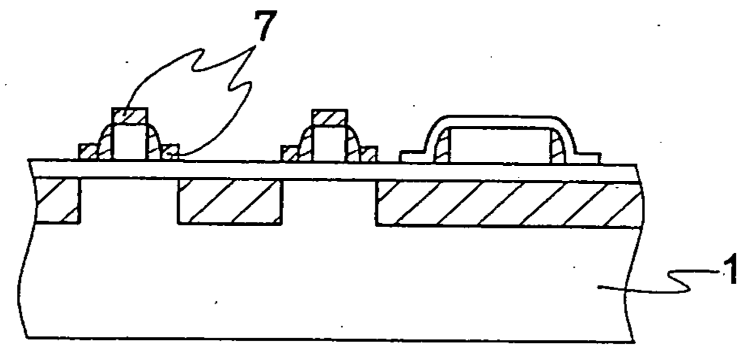


(c)

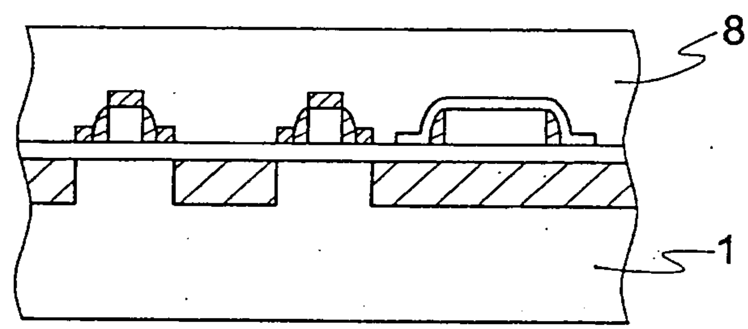


[Fig. 16]

(a)



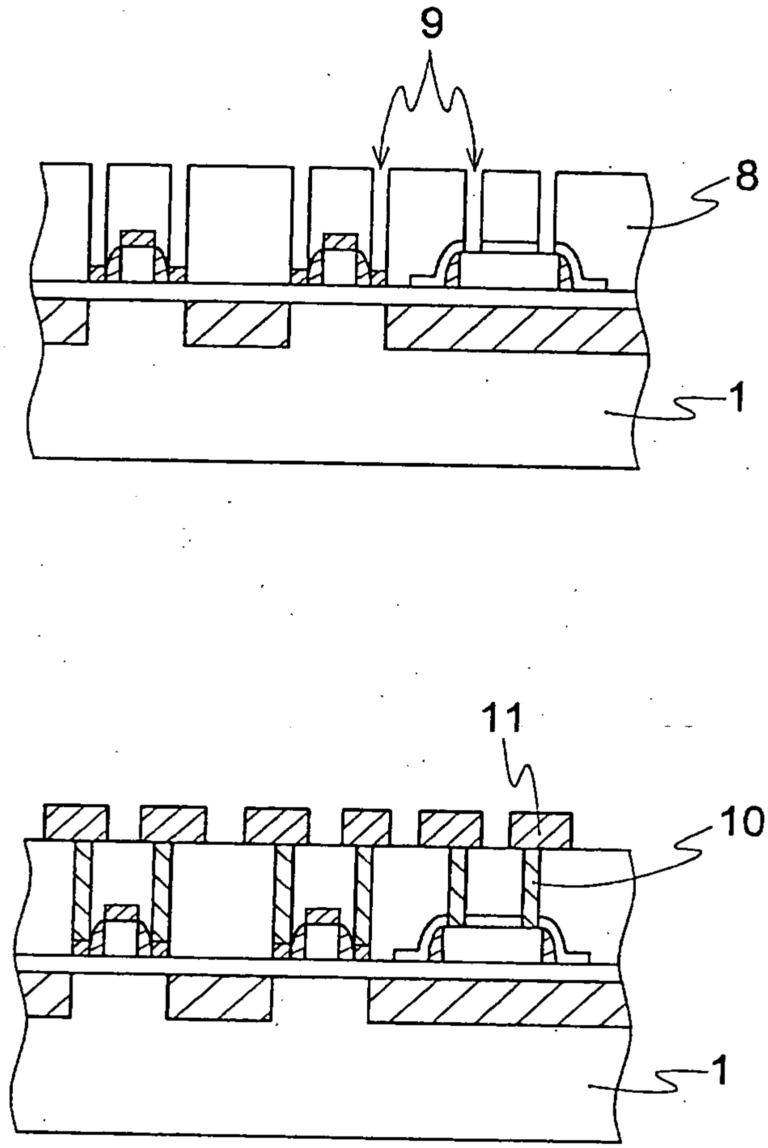
(b)



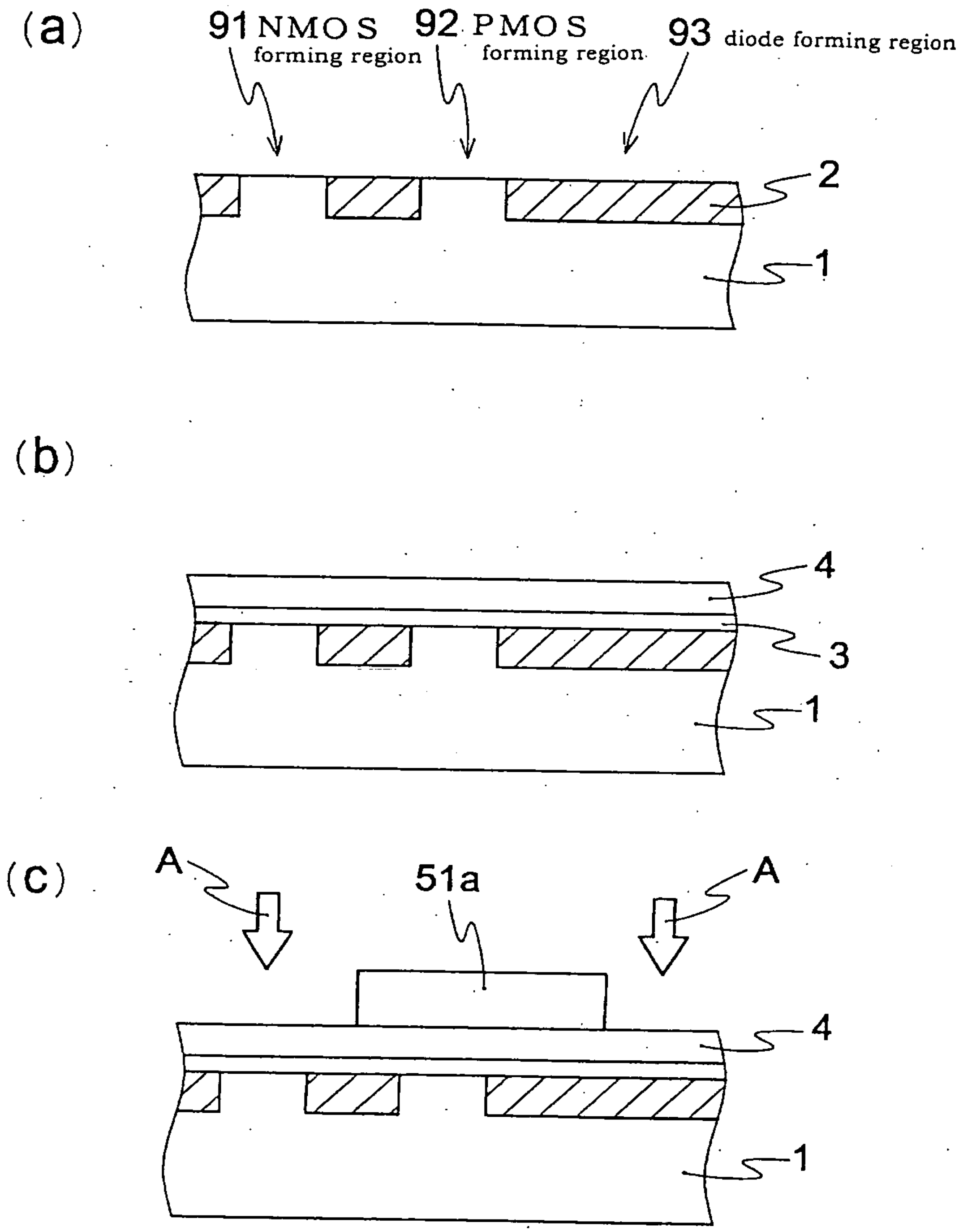
[Fig. 17]

(a)

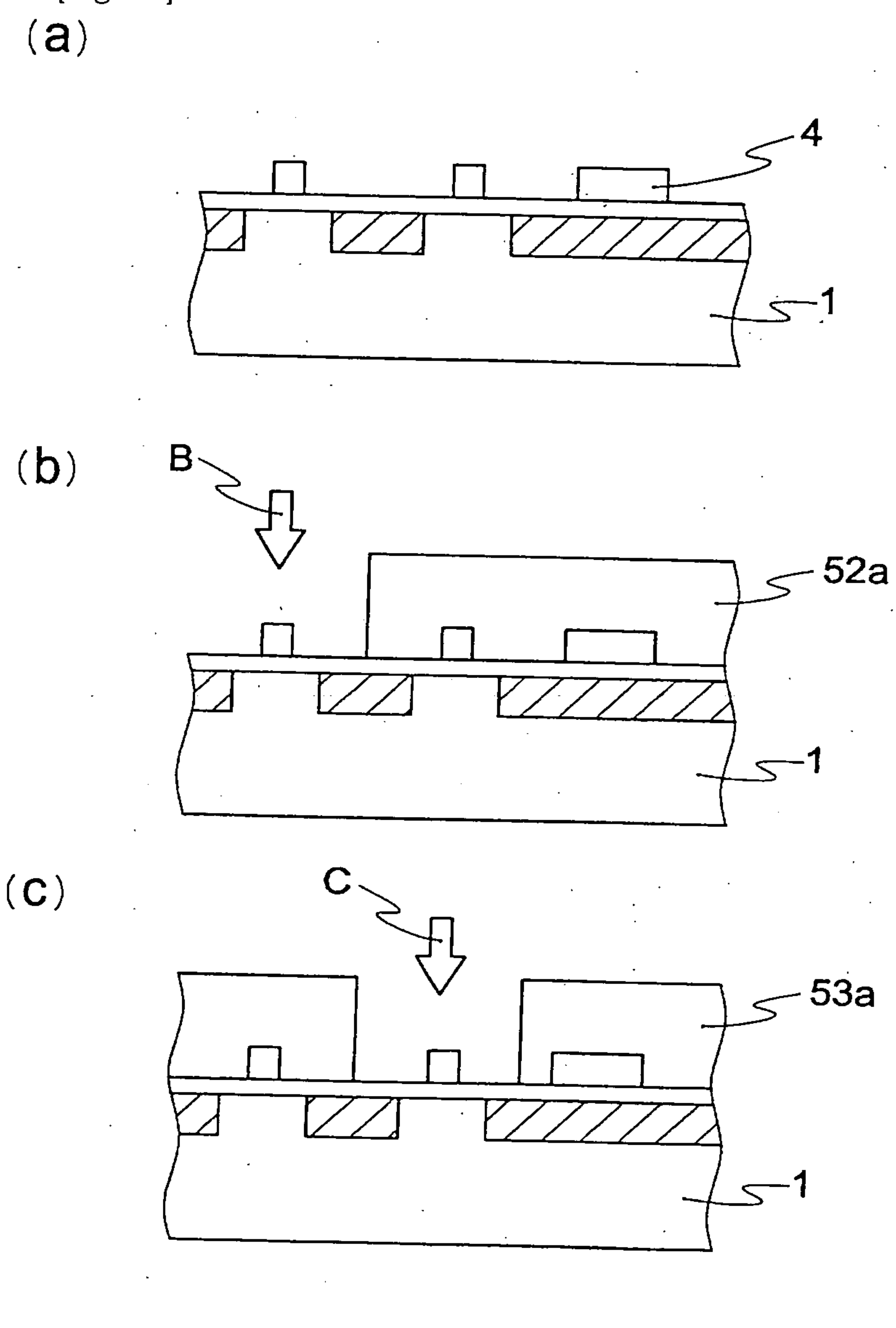
(b)



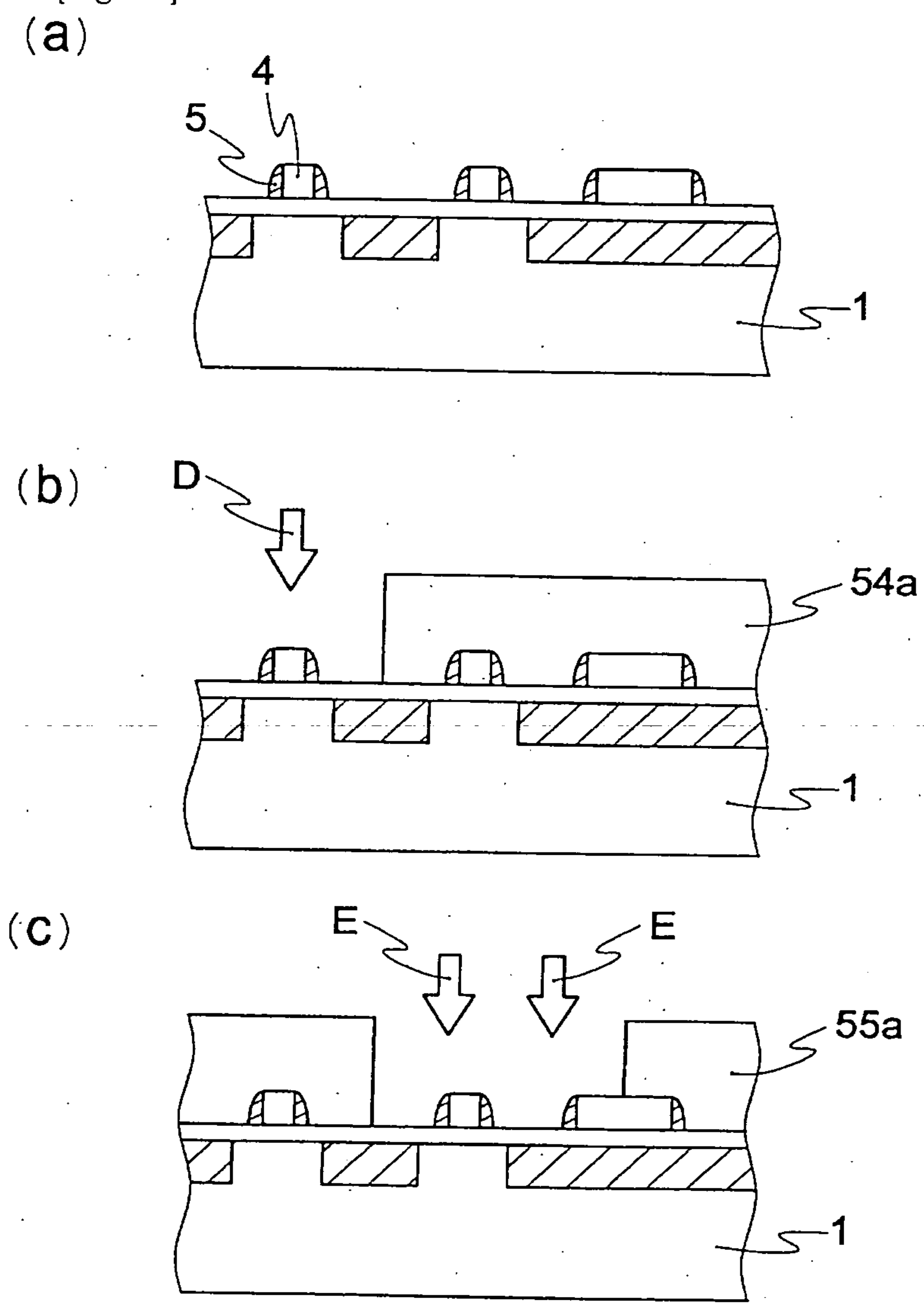
[Fig. 18]


(a)
91 NMOS forming region
92 PMOS forming region
93 diode forming region
2
1
(b)
4
3
1
(c)
A
51a
A
4
1

[Fig. 19]

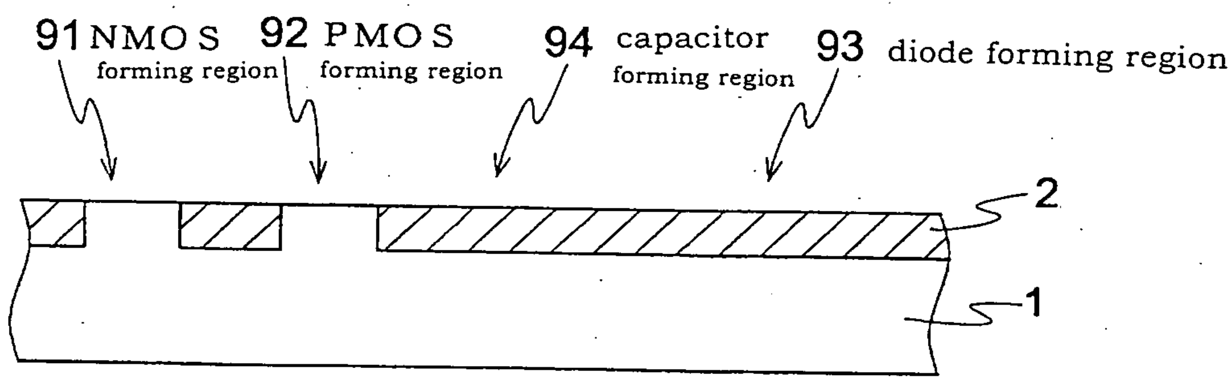


[Fig. 20]

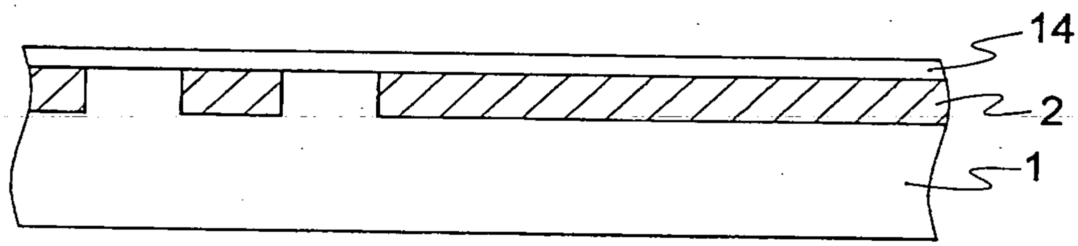


[Fig. 21]

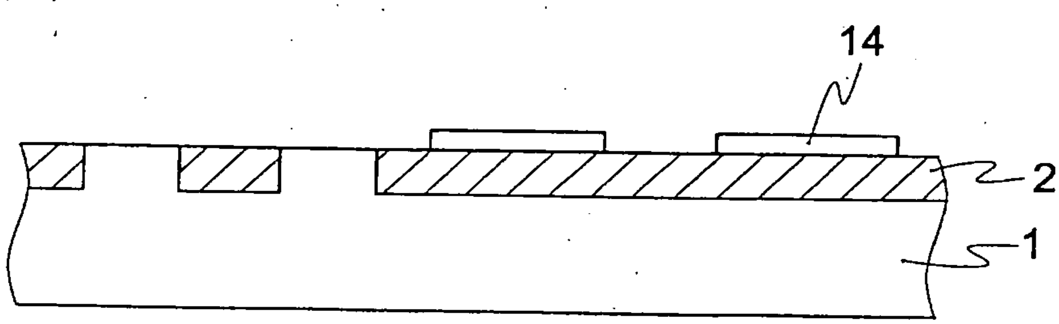
(a)


91 NMOS forming region
92 PMOS forming region
94 capacitor forming region
93 diode forming region
2
1

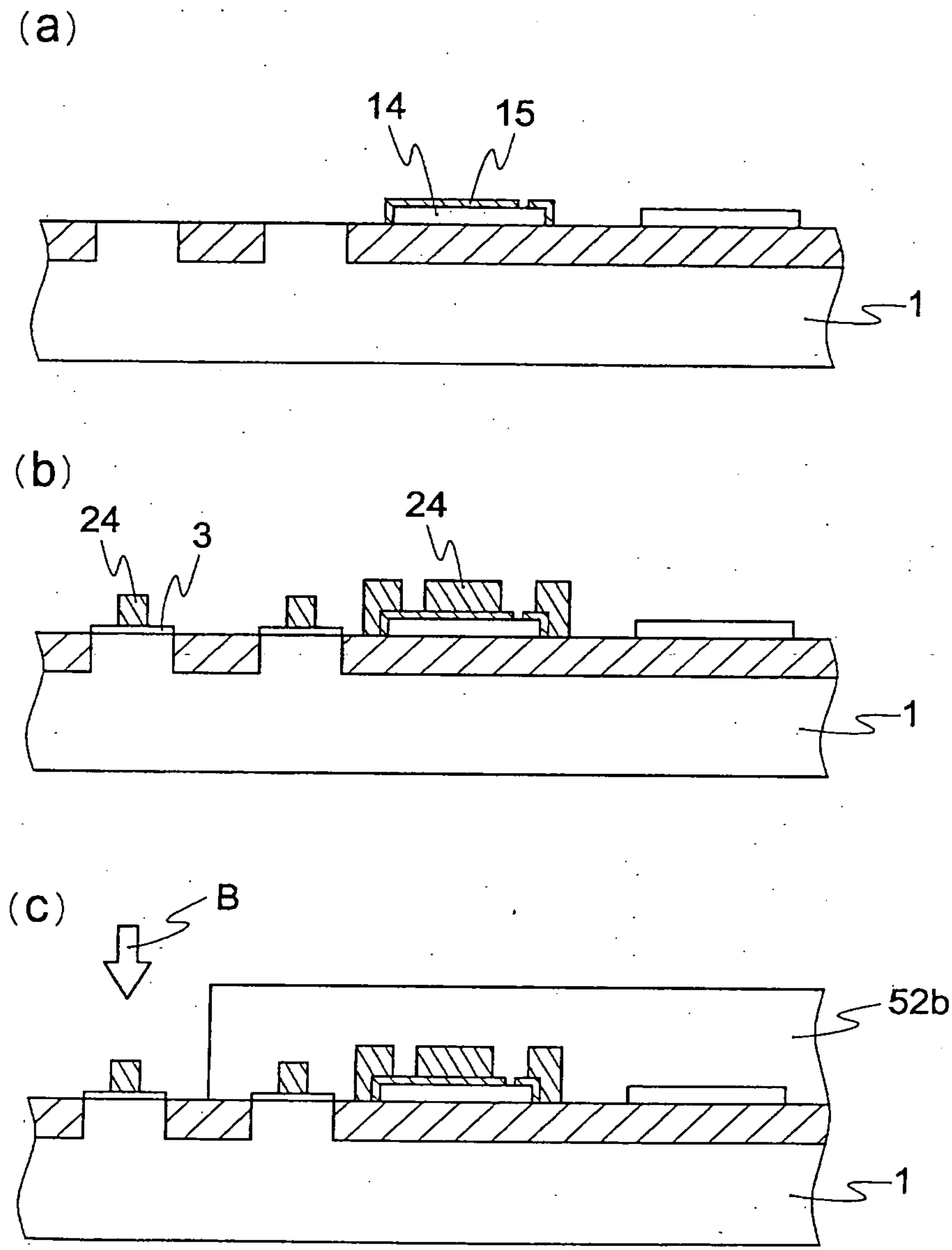
(b)


14
2
1

(c)

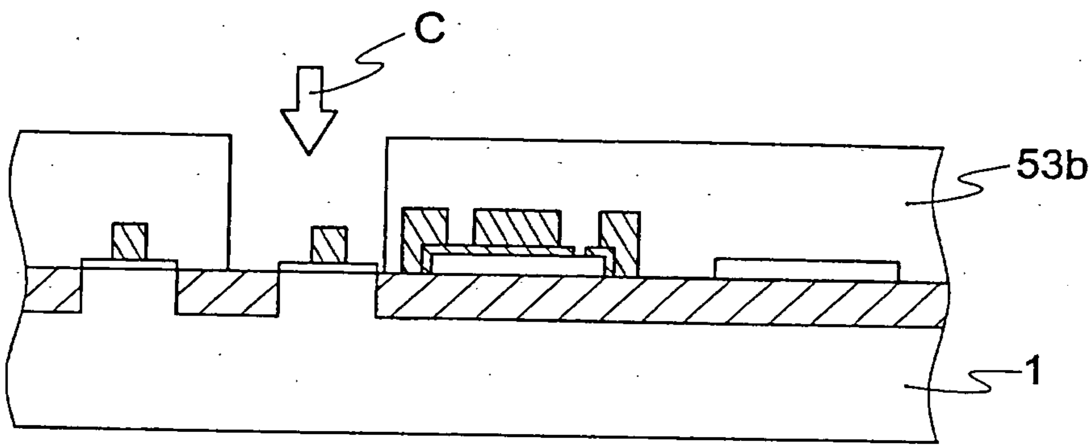

14
2
1

[Fig. 22]

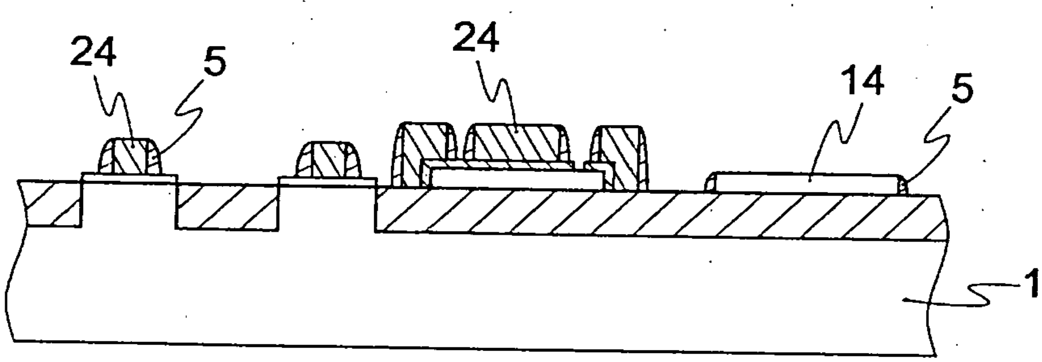


[Fig. 23]

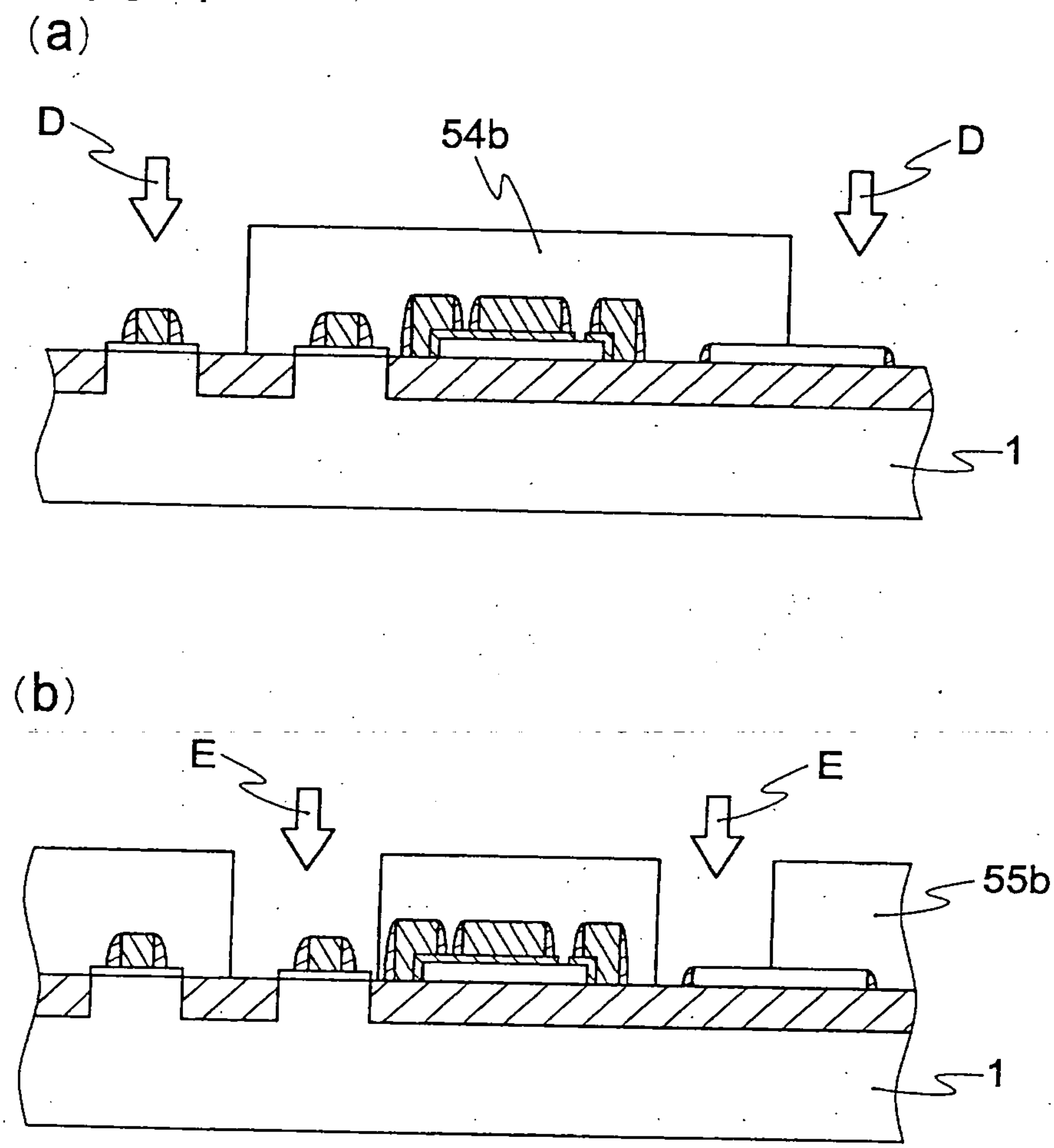
(a)



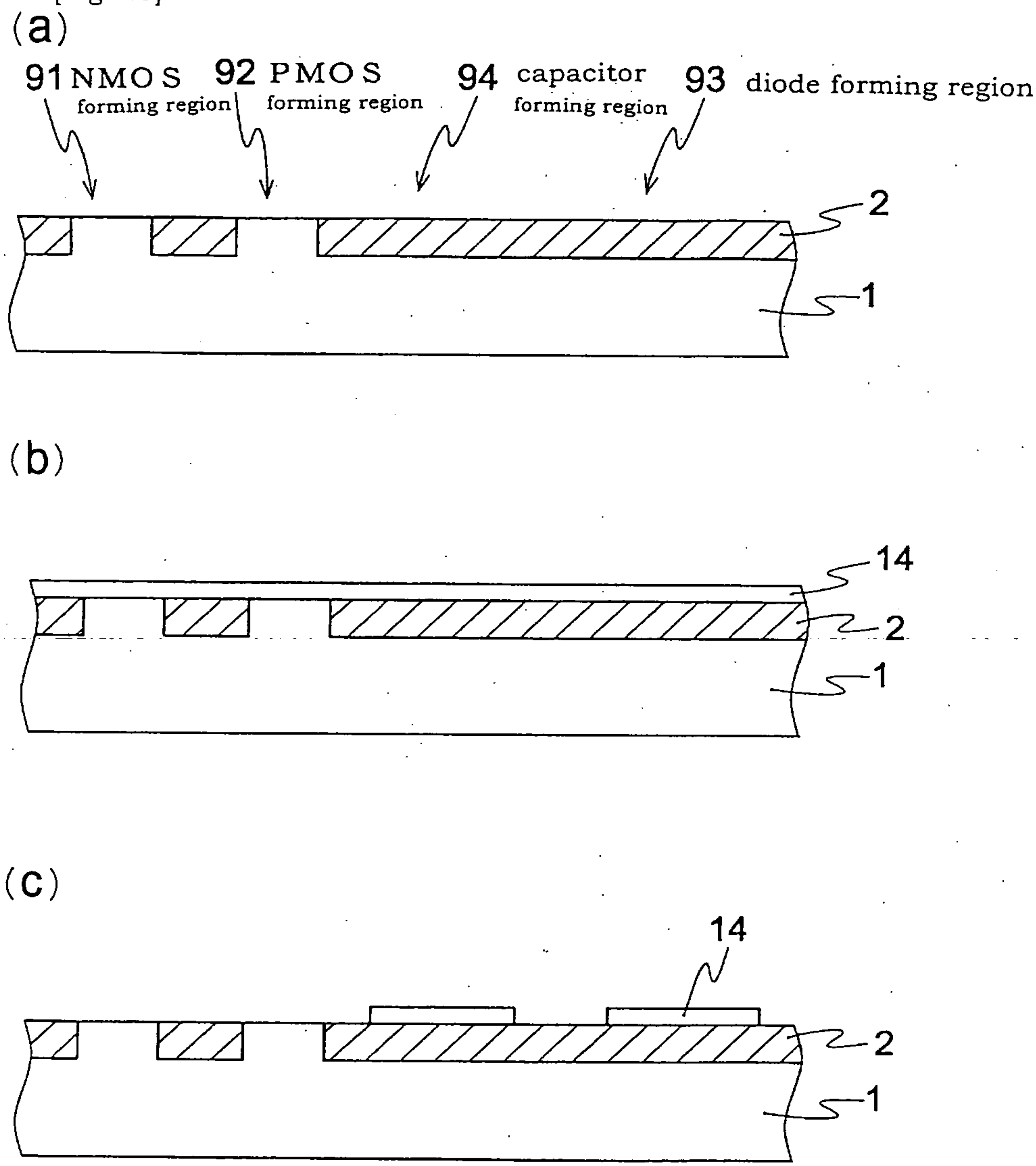
(b)



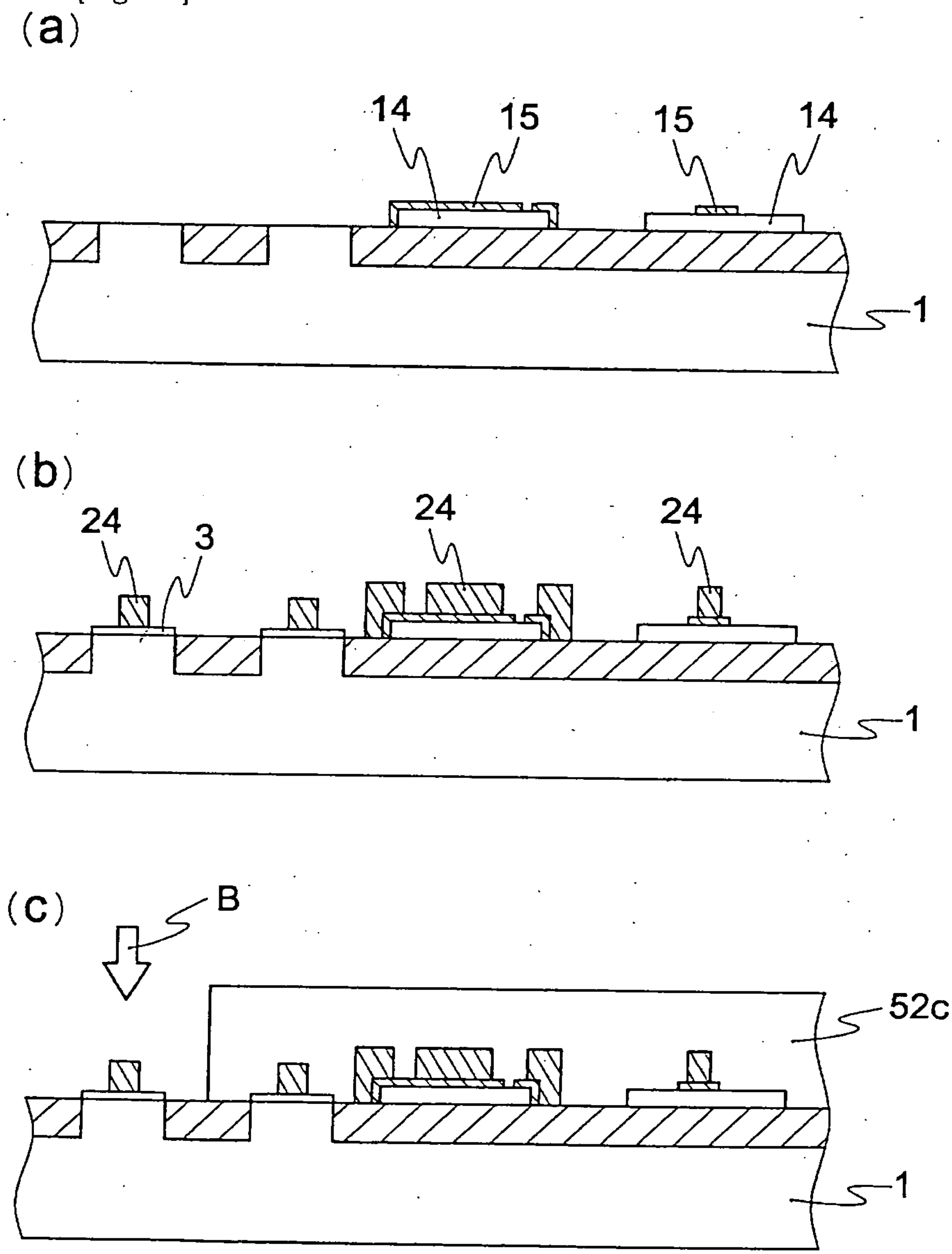
[Fig. 24]



[Fig. 25]

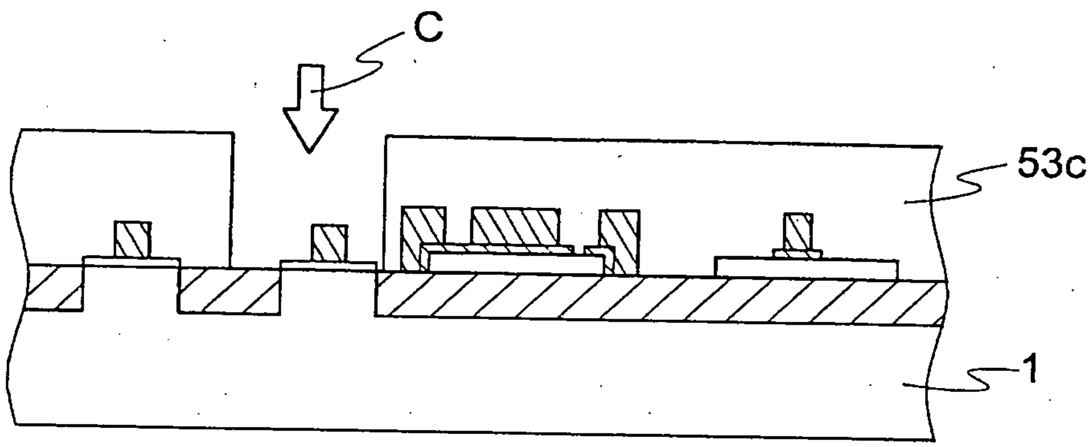

(a)
91 NMOS forming region
92 PMOS forming region
94 capacitor forming region
93 diode forming region
2
1
(b)
14
2
1
(c)
14
2
1

[Fig. 26]

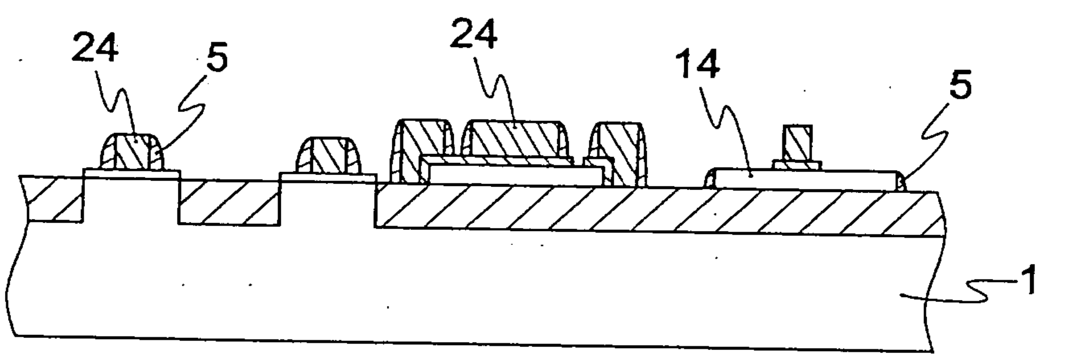


[Fig. 27]

(a)

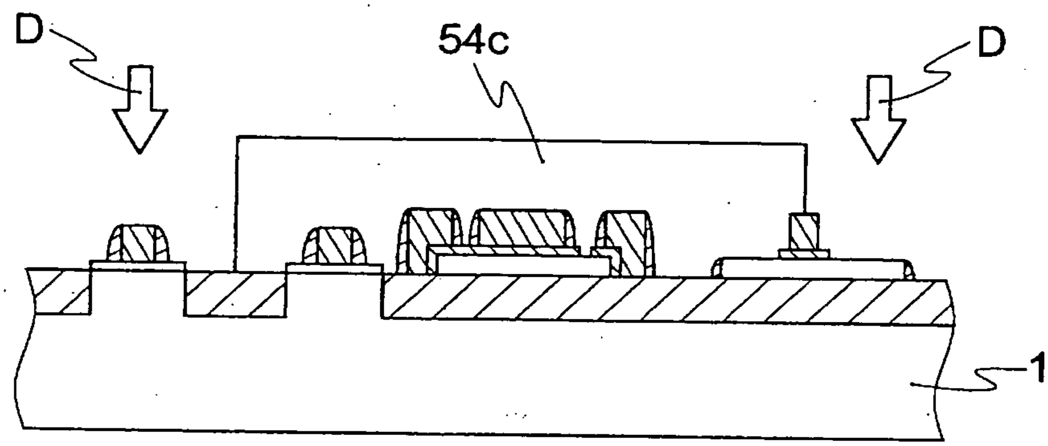


(b)

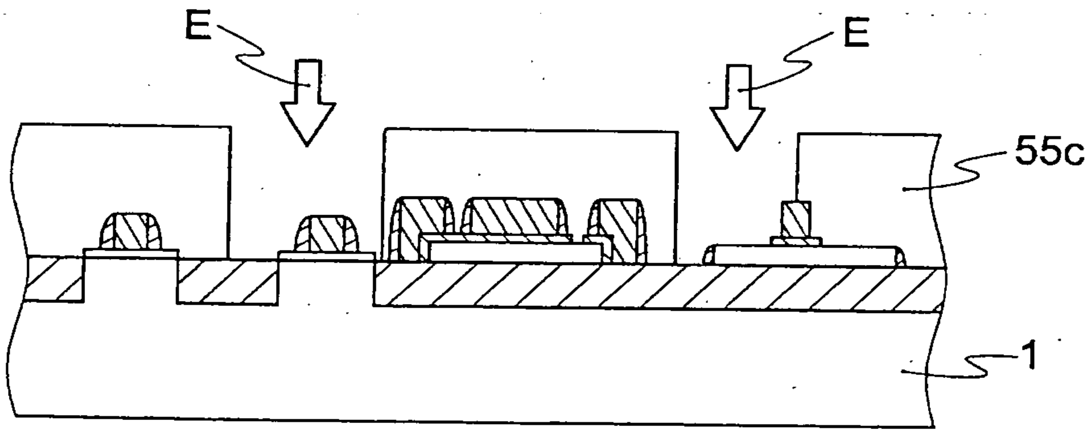


[Fig. 28]

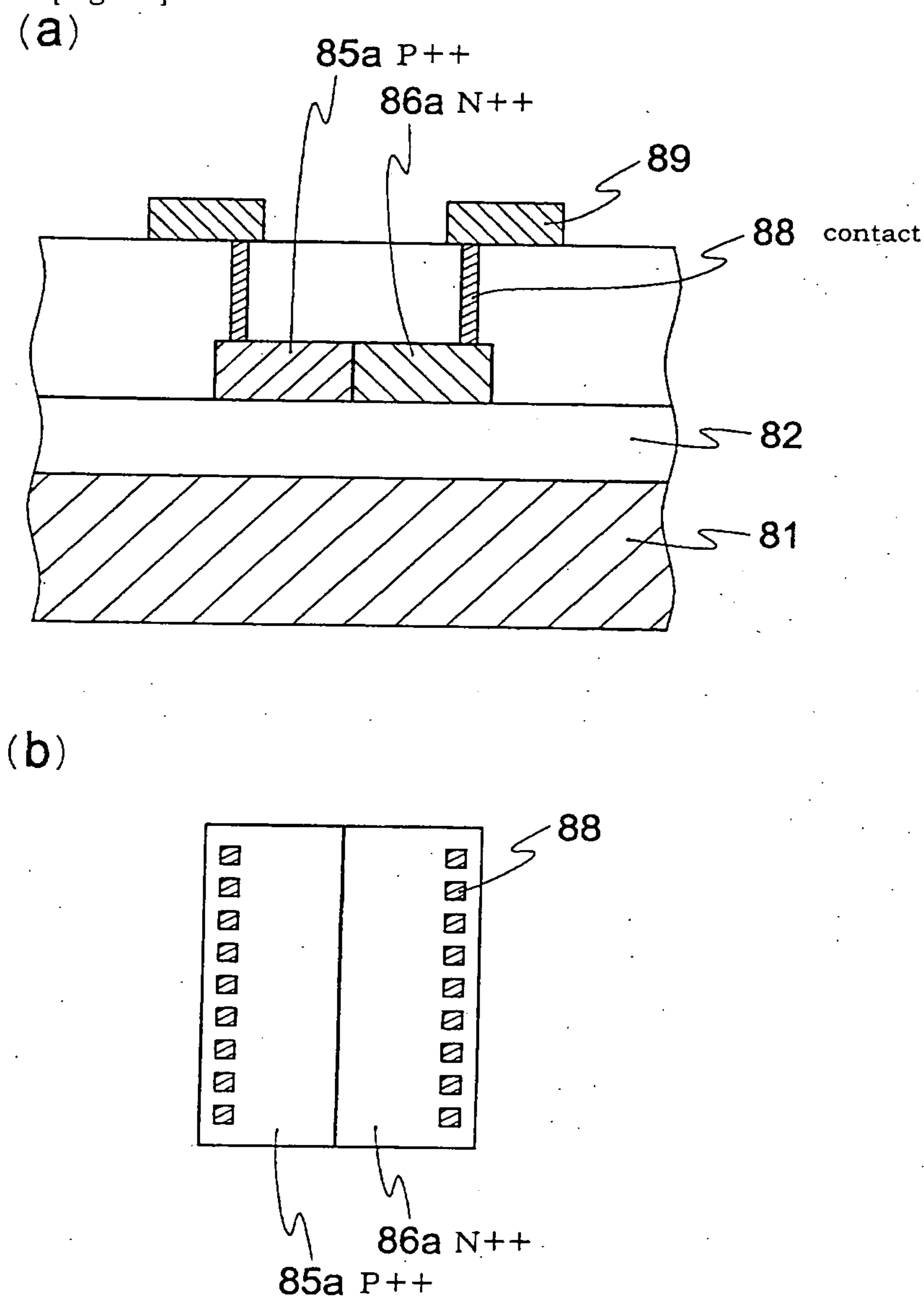
(a)



(b)

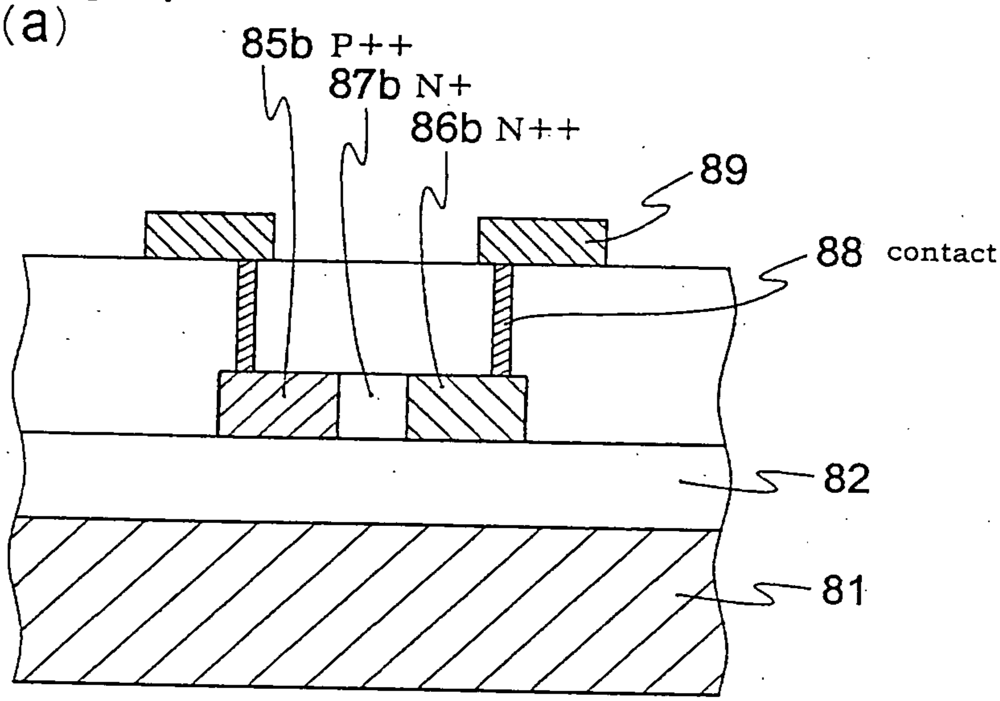


[Fig. 29]

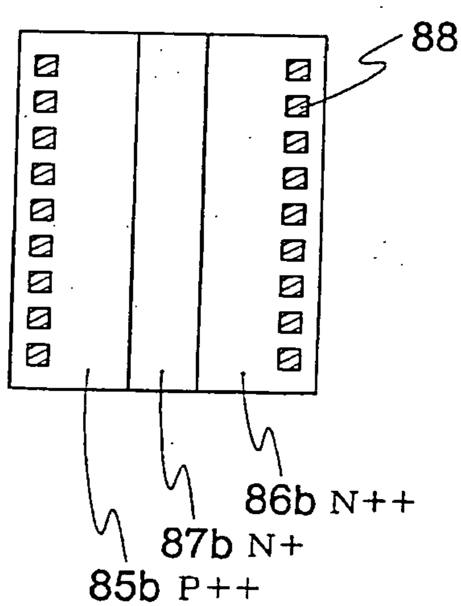


[Fig. 30]

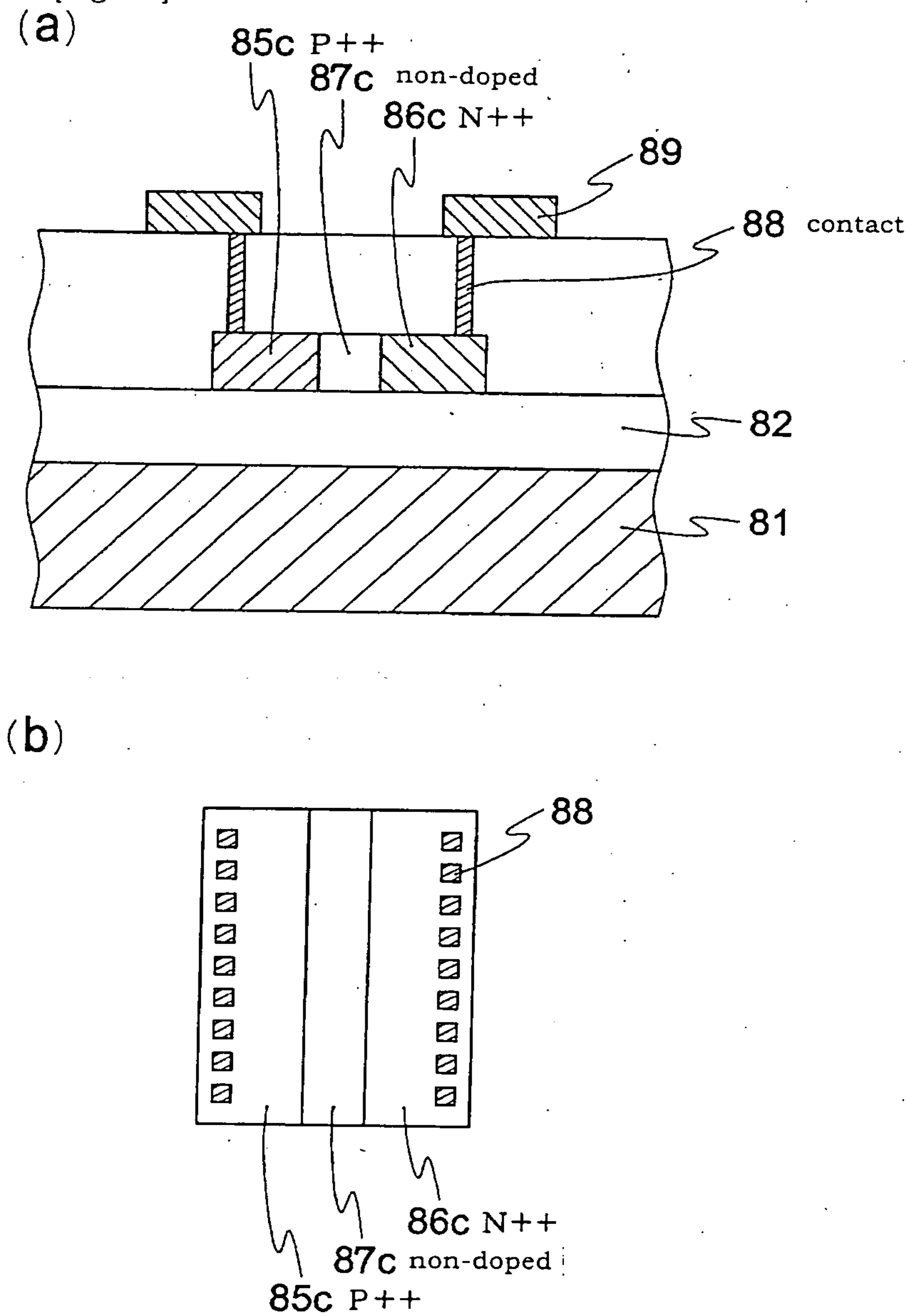
(a)



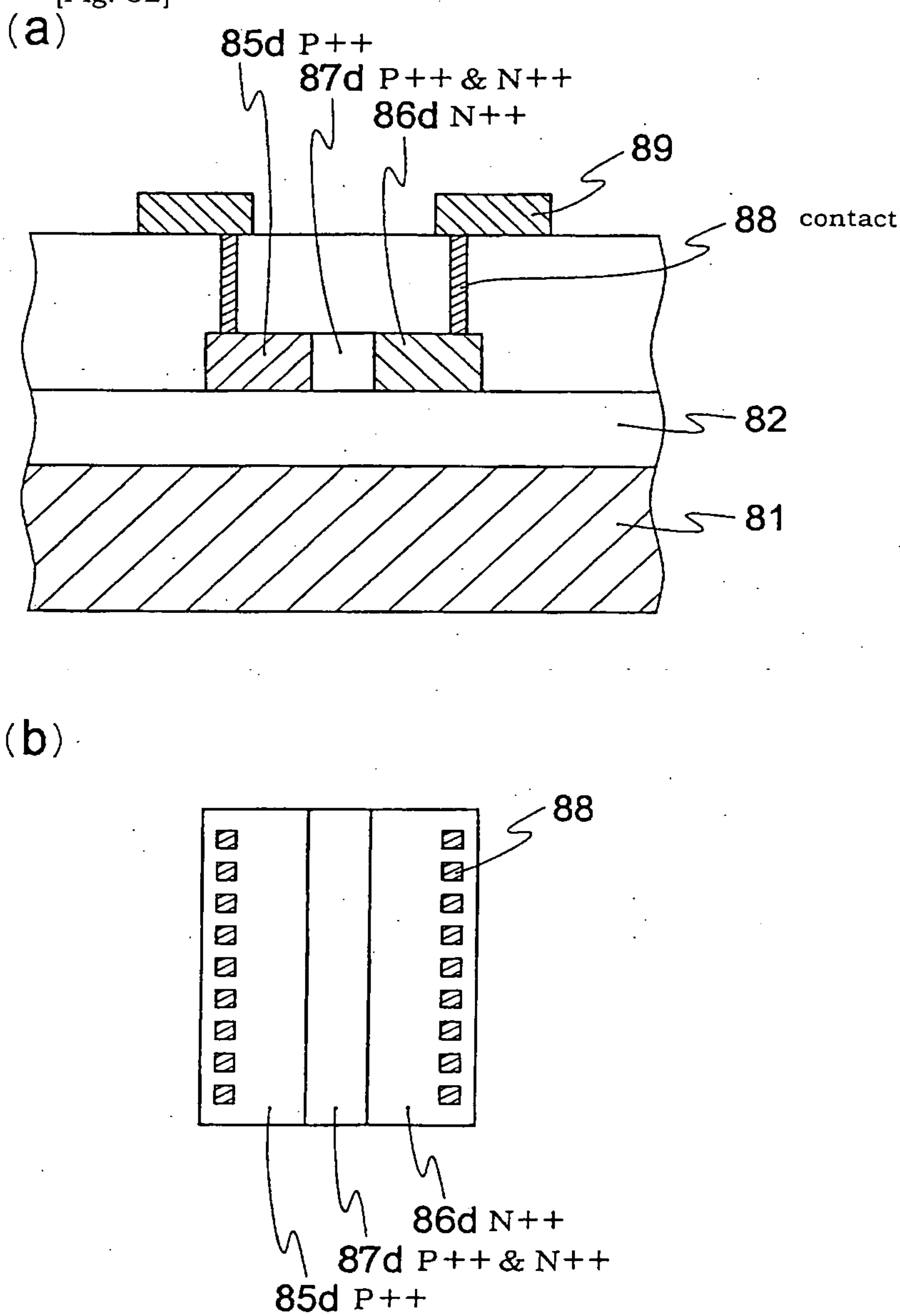
(b)



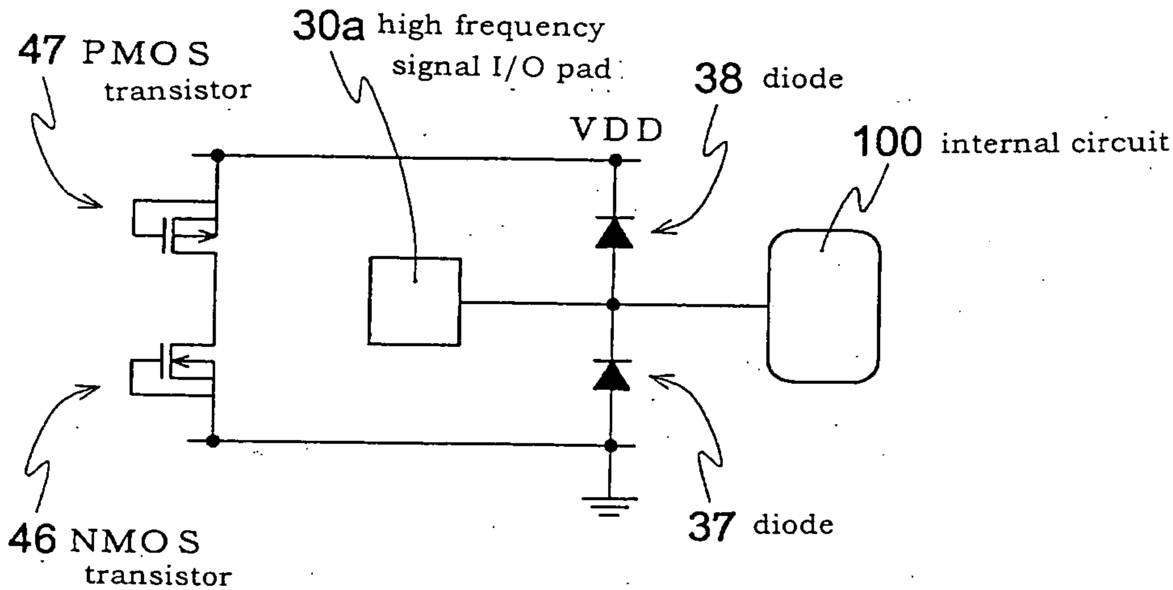
[Fig. 31]


(a)
85c P++
87c non-doped
86c N++
89
88 contact
82
81
(b)
88
86c N++
87c non-doped
85c P++

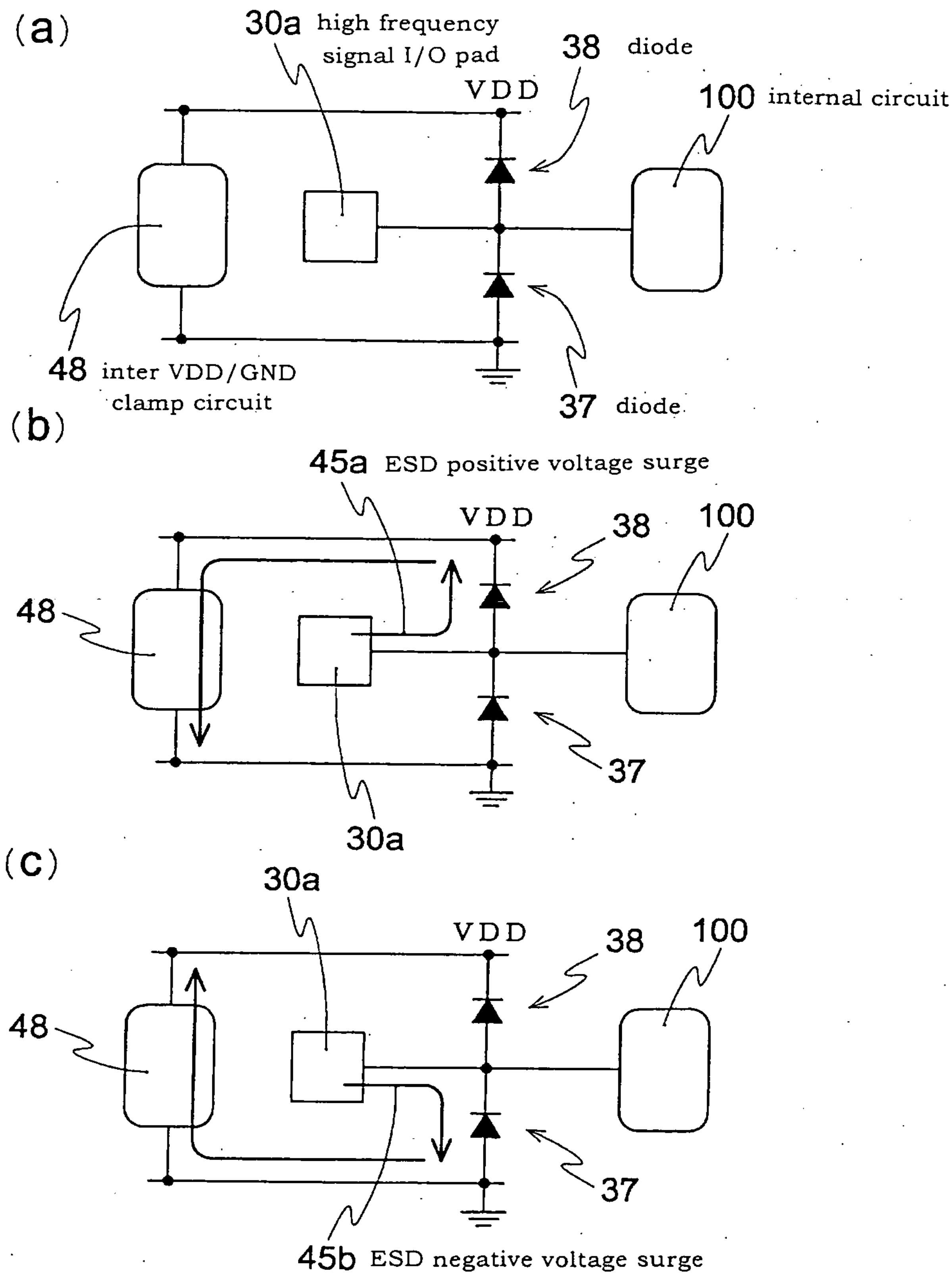
[Fig. 32]



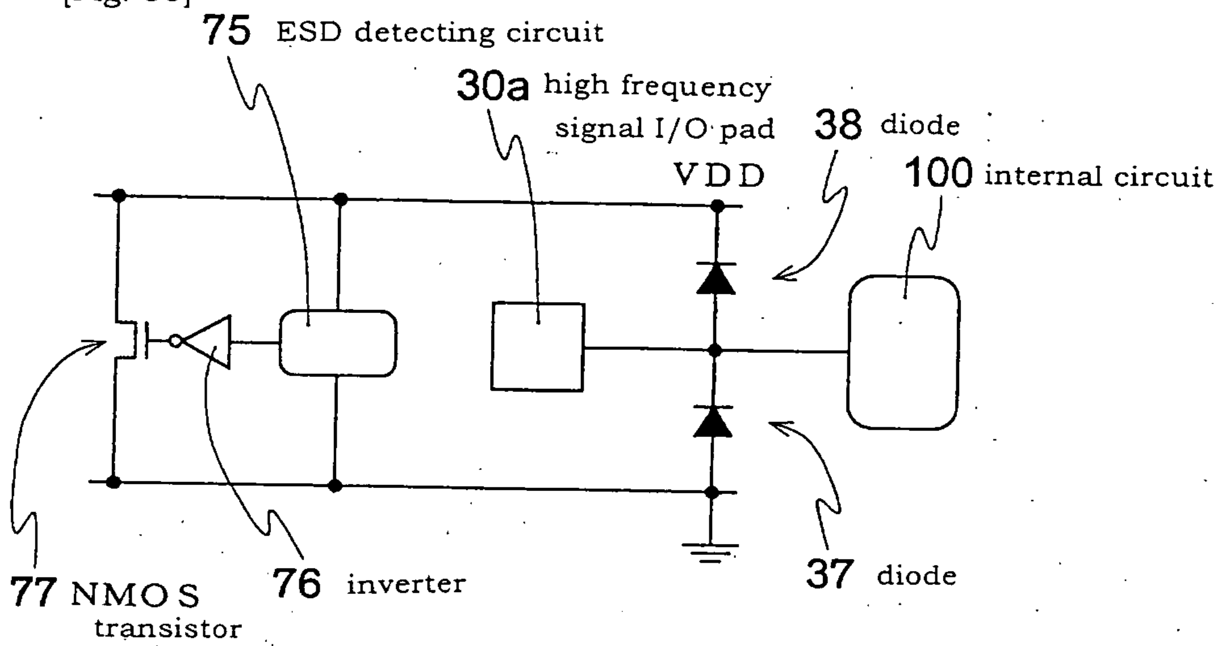
[Fig. 33]


47 PMOS transistor
30a high frequency signal I/O pad
38 diode
VDD
100 internal circuit
46 NMOS transistor
37 diode

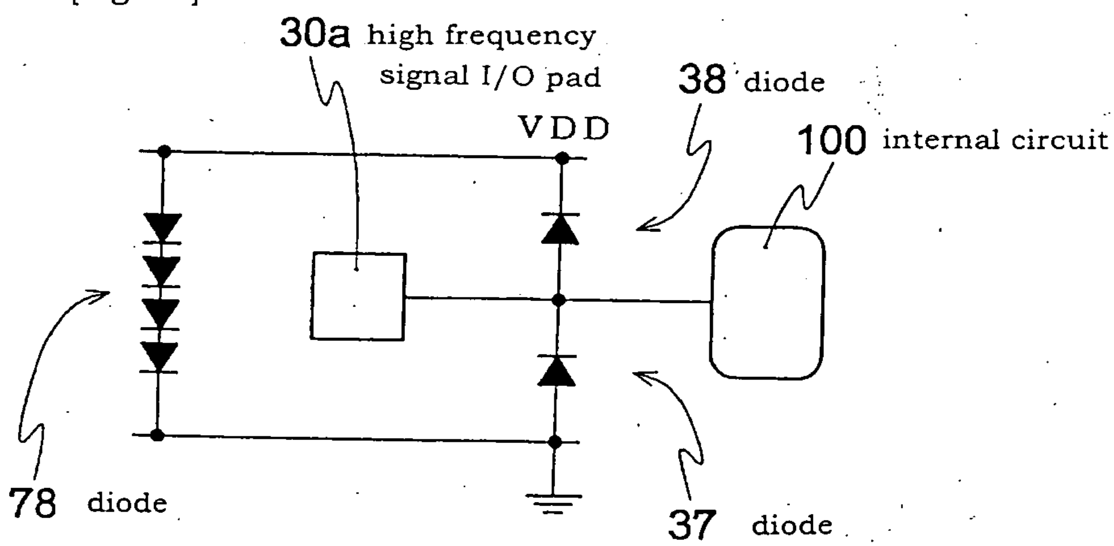
[Fig. 34]


(a)
30a high frequency signal I/O pad
38 diode
VDD
100 internal circuit
48 inter VDD/GND clamp circuit
37 diode
(b)
45a ESD positive voltage surge
VDD
38
100
48
37
30a
(c)
30a
VDD
38
100
48
37
45b ESD negative voltage surge

[Fig. 35]


75 ESD detecting circuit
30a high frequency signal I/O pad
38 diode
VDD
100 internal circuit
77 NMOS transistor
76 inverter
37 diode

[Fig. 36]


30a high frequency signal I/O pad
38 diode
VDD
100 internal circuit
78 diode
37 diode

[Document Name] ABSTRACT

[Abstract]

[Problem] An object of the present invention is to provide a sophisticated and highly reliable high-frequency Si-MOS semiconductor device having high ESD resistance.

[Solution] In the semiconductor device according to the present invention, lateral polysilicon diodes are formed and connected between high-frequency I/O signal line and the external supply voltage VDD, and between the ground GND and the high-frequency I/O signal line respectively. The forward direction of the diodes is the direction from the high-frequency I/O signal line to the VDD and the direction from the ground GND to the high-frequency I/O signal line respectively.

[Selected Figure] Figure 6